HY11P41
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 18-Bit ΣΔADC

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注意：

1、 本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com。

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3、 本產品在單獨應用的情況下，本公司保證它的性能、典型應用和功能符合說明書中的條件。當使用在客戶的產品或設備中，以上條件我們不作保證，建議客戶做充分的評估和測試。

4、 請注意輸入電壓、輸出電壓、負載電流的使用條件，使 IC 內的功耗不超過封裝的容許功耗。對於客戶在超出說明書中規定額定值使用產品，即使是瞬間的使用，由此所造成的損失，本公司不承擔任何責任。

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6、 本規格書中的產品，未經書面許可，不可使用在要求高可靠性的電路中。例如健康醫療器械、防災器械、車輛器械、車載器械及航空器械等對人體產生影響的器械或裝置，不得作為其部件使用。

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8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- 8 位元加強型精簡指令集，共有 66 個指令包含硬體乘法指令及查表指令
- 2.2V to 3.6V工作電壓範圍，-40℃~85℃工作溫度範圍
- 內部高精度RC震盪器，4 種CPU工作時脈切換選擇，可讓使用者達到最佳省電規劃
  - 運行模式 300uA@2MHz
  - 待機模式 3uA@28KHz
  - 休眠模式 1uA
- 2KWord OTP (One Time Programmable) Type程式記憶體，128Byte資料記憶體
- Brownout and Watch dog Timer，可防止CPU進入死機模式
- 18bit 全差動輸入ΣΔADC類比數位轉換器
  - 內置(Programmable Gain Amplifier)及可有 1/4、1/2、1. …..128 倍 10 種輸入信號放大倍率選擇
  - 內置輸入零點調整，可針對不同應用增加其量測範圍
  - 可程式設定 8SPS到 2K SPS的數據輸出速率
  - 內置絕對溫度感測器
- 1.0V, 1.2V的內部類比電路共地電壓源，具有Push-Pull驅動能力，可提供傳感器驅動電壓
- LVD低電壓檢測功能具 14 段檢測電壓設置與外部輸入電壓檢測功能
- 類比電壓源VDDA可選擇 4 種不同輸出電壓，具 10mA穩壓電壓源輸出能力及快速啓動功能
- 8-bit Timer A
- 16-bit Timer B模組具Capture 功能
- 8-bit Timer C 模組具PWM/PFD波形產生功能
- Build-In EPROM (BIE)
- Support 6 stack level

功能列表

Model No.	VDD	System Clock	Program Memory (word)	SRAM (byte)	BIE (word)	ADC ENOB (bit x ch)	Sample Rate (sps)	TPS	I/O	Timer (bit x ch)	PWM (bit x ch)	Package
HY11P41	2.2V~3.6V	28KHz~2MHz	2K	128	64	20-bit x 4	8~1953	yes	8xI + 5xIO	8-bit x 2 16-bit x 1	8-bit x 1	SSOP16 SOP16 QFN16

2. 引腳定義

2.1. SSOP16 引腳圖

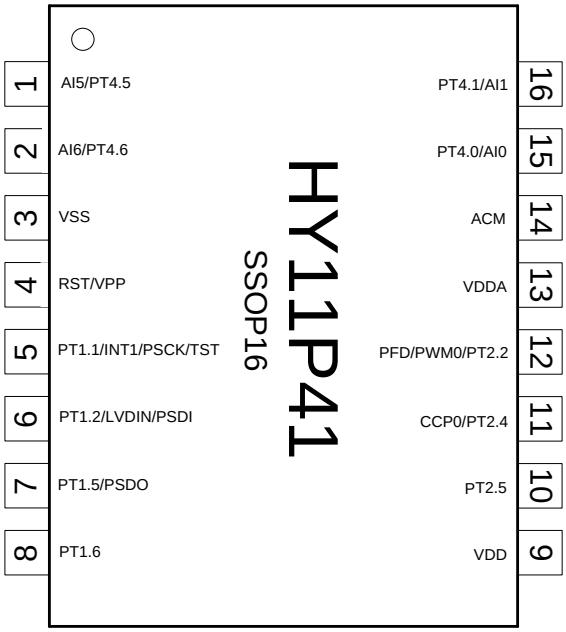


圖 2-1 HY11P41 SSOP16 引腳圖

2.2. SOP16 引腳圖

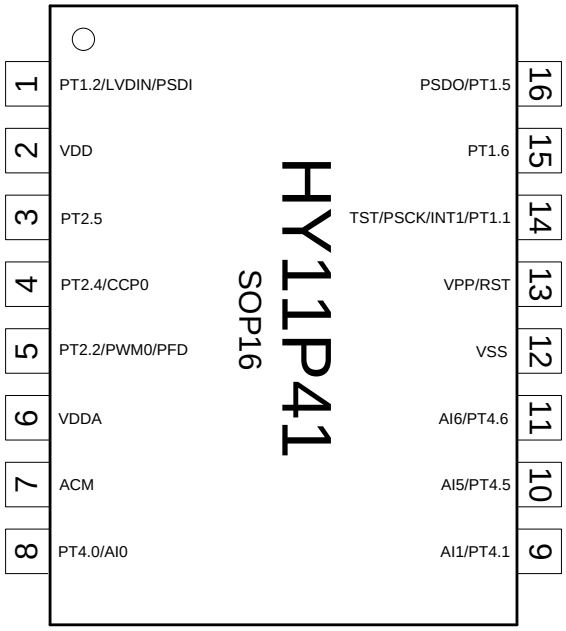


圖 2-2 HY11P41 SOP16 引腳圖

2.3. QFN16 引腳圖

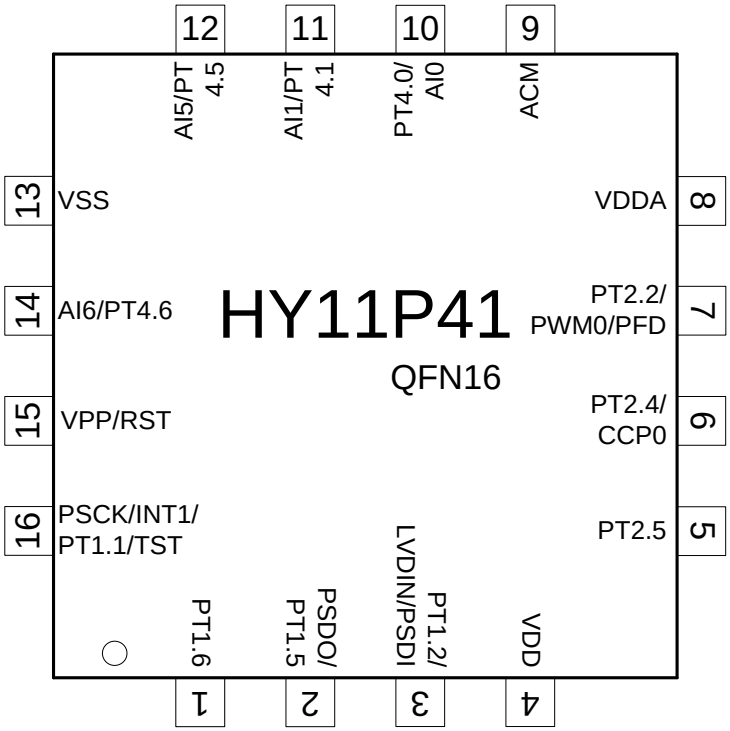


圖 2-3 HY11P41 QFN16 引腳圖

註 1：VPP 與 RST 復用同一接口，非燒錄 EPROM 時禁止輸入電壓超過 5.8V

註 2：TST 與 PT1.1 復用同一接口，操作時禁止輸入電壓超過 VDD+0.3V

註 3：若不將 PT1.1 設定成外部引腳按鍵，可以提升抗干擾能力

2.4. I/O 引腳定義(SSOP16)

"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS 特性兼容輸出與輸入,"P"電壓源,"A"類比通道

編號	引腳名稱	引腳特性		功能說明
		格式	緩衝	
1	AI5/PT4.5 AI5 PT4.5	 A I	 A C	 類比輸入通道入 數位輸 入
2	AI6/PT4.6 AI6 PT4.6	 A I	 A C	 類比輸入通道 數位輸入
3	VSS	P	P	晶片工作電壓源接地端
4	RST/VPP RST VPP	 I P	 S P	 復位晶片 EPROM讀/寫時的電壓源
5	PT1.1/INT1/PSCK/TST PT1.1 INT1 PSCK TST	 I I I I	 S S S S	 數位輸入 中斷源INT1 OTP讀/寫介面PSCK接口 測試模式致能輸入（未開放）
6	PT1.2/LVDIN/PSDI PT1.2 LVDIN PSDI	 I A I	 S A S	 數位輸入 LVD 外部信號輸入接口 OTP讀/寫介面PSDI接口
7	PT1.5/PSDO PT1.5 PSDO	 I/O I/O	 S C	 數位輸入/輸出 OTP讀/寫介面PSDO接口
8	PT1.6 PT1.6	 I/O	 S	 數位輸入/輸出
9	VDD	P	P	晶片工作電壓源
10	PT2.5 PT2.5	 I/O	 S	 數位輸入/輸出
11	PT2.4/CCP0 PT2.4 CCP0	 I/O I	 S S	 數位輸入/輸出 捕捉模式信號接口
12	PT2.2/PWM0/PFD PT2.2 PWM0 PFD	 I/O O O	 C C C	 數位輸入/輸出 PWM 輸出接口 PFD 輸出接口
13	VDDA	P	P	穩壓器輸出，類比電路電壓源
14	ACM	P	P	內部類比電路共地引腳
15	AI0/PT4.0 AI0 PT4.0	 A I	 A C	 類比輸入通道 數位輸入
16	AI1/PT4.1 AI1 PT4.1	 A I	 A C	 類比輸入通道 數位輸入

表 2-1 引腳定義與功能說明

2.5. I/O 引腳定義(SOP16)

"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS 特性兼容輸出與輸入,"P"電壓源,"A"類比通道

編號	引腳名稱	引腳特性		功能說明
		格式	緩衝	
1	PT1.2/LVDIN/PSDI PT1.2 LVDIN PSDI	 I A I	 S A S	 數位輸入 LVD 外部信號輸入接口 OTP讀/寫介面PSDI接口
2	VDD	P	P	晶片工作電壓源
3	PT2.5 PT2.5	 I/O	 S	 數位輸入/輸出
4	PT2.4/CCP0 PT2.4 CCP0	 I/O I	 S S	 數位輸入/輸出 捕捉模式信號接口
5	PT2.2/PWM0/PFD PT2.2 PWM0 PFD	 I/O O O	 C C C	 數位輸入/輸出 PWM 輸出接口 PFD 輸出接口
6	VDDA	P	P	穩壓器輸出，類比電路電壓源
7	ACM	P	P	內部類比電路共地引腳
8	AI0/PT4.0 AI0 PT4.0	 A I	 A C	 類比輸入通道 數位輸入
9	AI1/PT4.1 AI1 PT4.1	 A I	 A C	 類比輸入通道 數位輸入
10	AI5/PT4.5 AI5 PT4.5	 A I	 A C	 類比輸入通道入 數位輸 入
11	AI6/PT4.6 AI6 PT4.6	 A I	 A C	 類比輸入通道 數位輸入
12	VSS	P	P	晶片工作電壓源接地端
13	RST/VPP RST VPP	 I P	 S P	 復位晶片 EPROM讀/寫時的電壓源
14	PT1.1/INT1/PSCK/TST PT1.1 INT1 PSCK TST	 I I I I	 S S S S	 數位輸入 中斷源INT1 OTP讀/寫介面PSCK接口 測試模式致能輸入（未開放）
15	PT1.6 PT1.6	 I/O	 S	 數位輸入/輸出
16	PT1.5/PSDO PT1.5 PSDO	 I/O I/O	 S C	 數位輸入/輸出 OTP讀/寫介面PSDO接口

表 2-2 引腳定義與功能說明

2.6. I/O 引腳定義(QFN16)

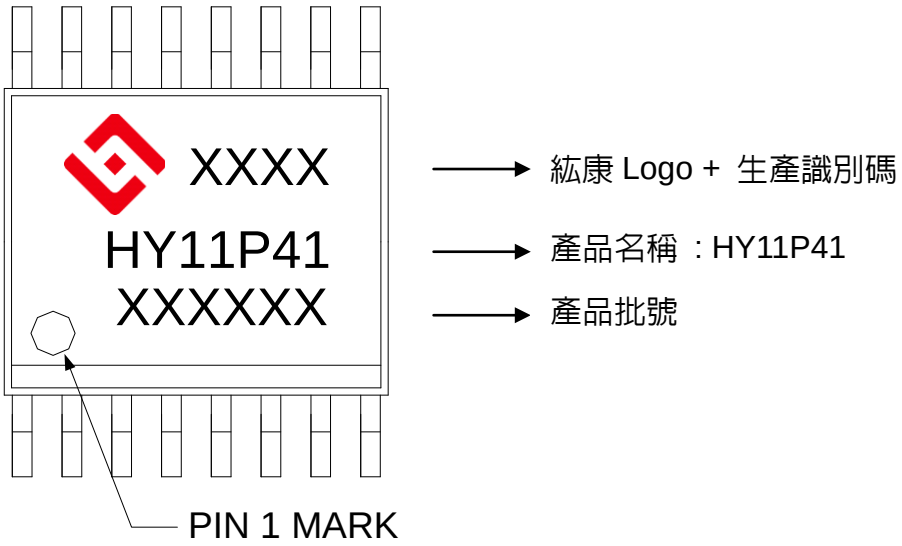
"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS 特性兼容輸出與輸入,"P"電壓源,"A"類比通道

編號	引腳名稱	引腳特性		功能說明
		格式	緩衝	
1	PT1.6 PT1.6	 I/O	 S	 數位輸入/輸出
2	PT1.5/PSDO PT1.5 PSDO	 I/O I/O	 S C	 數位輸入/輸出 OTP讀/寫介面PSDO接口
3	PT1.2/LVDIN/PSDI PT1.2 LVDIN PSDI	 I A I	 S A S	 數位輸入 LVD 外部信號輸入接口 OTP讀/寫介面PSDI接口
4	VDD	P	P	晶片工作電壓源
5	PT2.5 PT2.5	 I/O	 S	 數位輸入/輸出
6	PT2.4/CCP0 PT2.4 CCP0	 I/O I	 S S	 數位輸入/輸出 捕捉模式信號接口
7	PT2.2/PWM0/PFD PT2.2 PWM0 PFD	 I/O O O	 C C C	 數位輸入/輸出 PWM 輸出接口 PFD 輸出接口
8	VDDA	P	P	穩壓器輸出，類比電路電壓源
9	ACM	P	P	內部類比電路共地引腳
10	AI0/PT4.0 AI0 PT4.0	 A I	 A C	 類比輸入通道 數位輸入
11	AI1/PT4.1 AI1 PT4.1	 A I	 A C	 類比輸入通道 數位輸入
12	AI5/PT4.5 AI5 PT4.5	 A I	 A C	 類比輸入通道入 數位輸 入
13	VSS	P	P	晶片工作電壓源接地端
14	AI6/PT4.6 AI6 PT4.6	 A I	 A C	 類比輸入通道 數位輸入
15	RST/VPP RST VPP	 I P	 S P	 復位晶片 EPROM讀/寫時的電壓源
16	PT1.1/INT1/PSCK/TST PT1.1 INT1 PSCK TST	 I I I I	 S S S S	 數位輸入 中斷源INT1 OTP讀/寫介面PSCK接口 測試模式致能輸入（未開放）

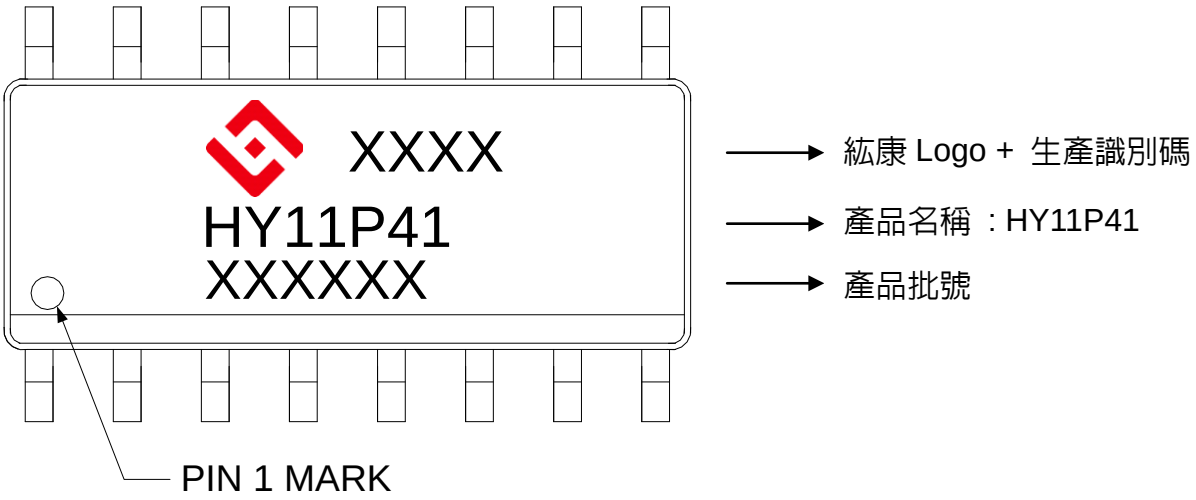
表 2-3 引腳定義與功能說明

2.7. 封裝片標記信息

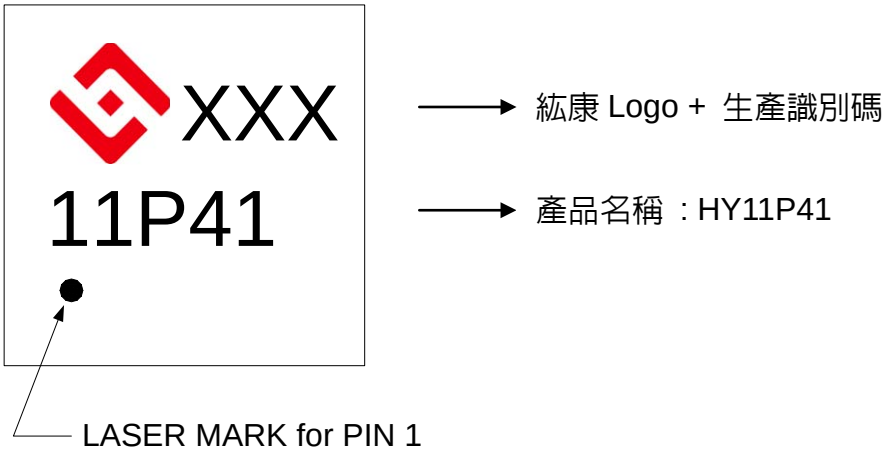
2.7.1. SSOP16 封裝片



2.7.2. SOP16 封裝片



2.7.3. QFN16 封裝片



3. 應用電路

3.1. 橋式感測器 I

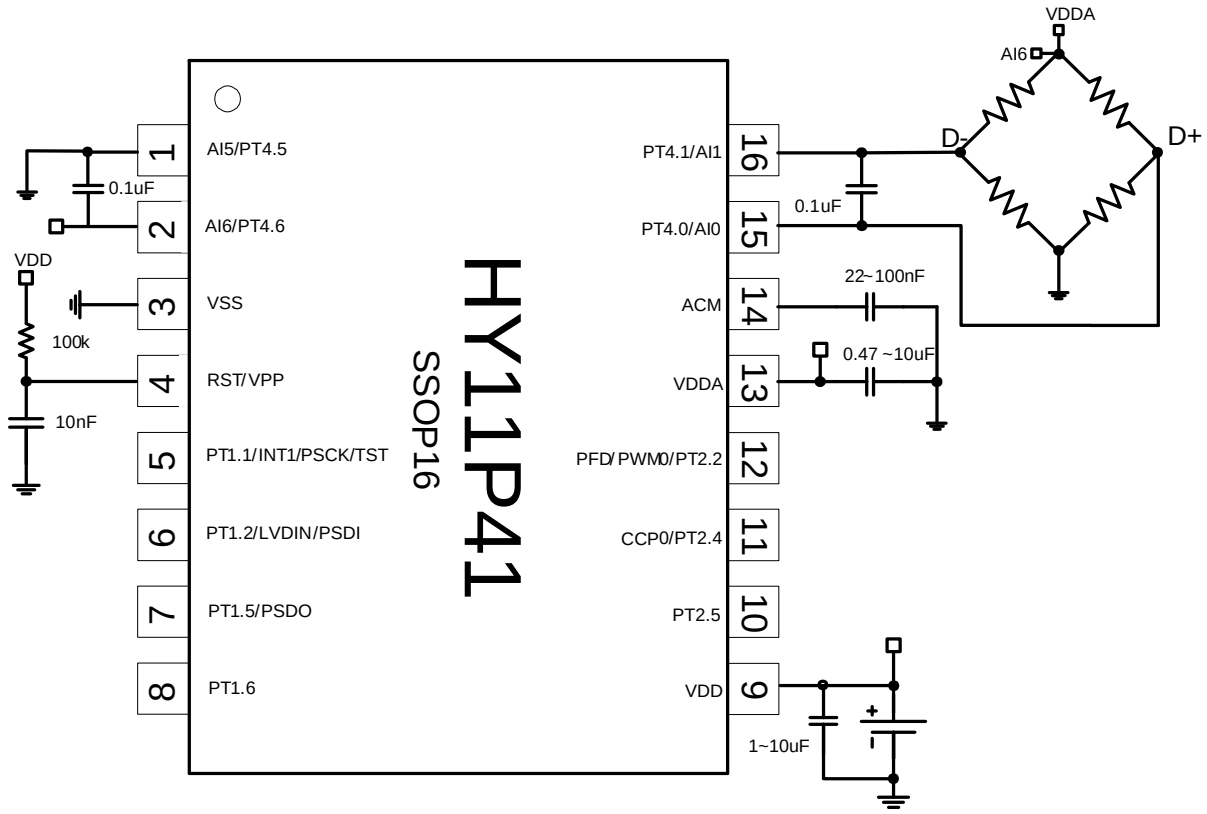


圖 3-1 橋式感測器應用電路

註 1：零點電壓位置可透過 DCSET[2:0]進行偏壓調整

註 2：校正參數儲存可使用 BIE 功能取代之

3.2. 橋式感測器 Ⅱ

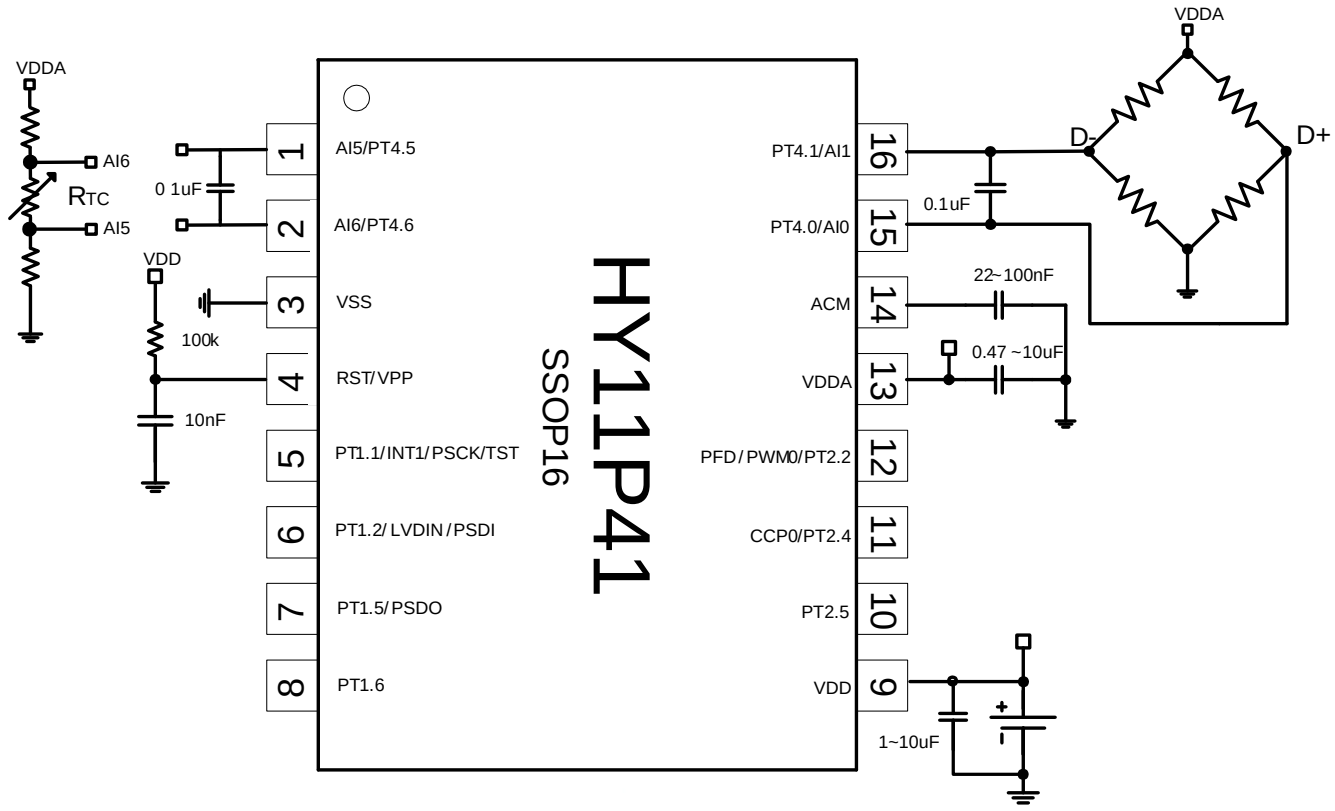


圖 3-2 具溫度補償的橋式感測器應用電路

註 1：使用溫度補償電阻 NTC 基本線路

註 2：關於零點電壓位置可透過 DCSET[2:0]進行偏壓調整

註 3：校正參數儲存可使用 BIE 功能取代之

3.3. 4-20mA 兩線式電流表頭

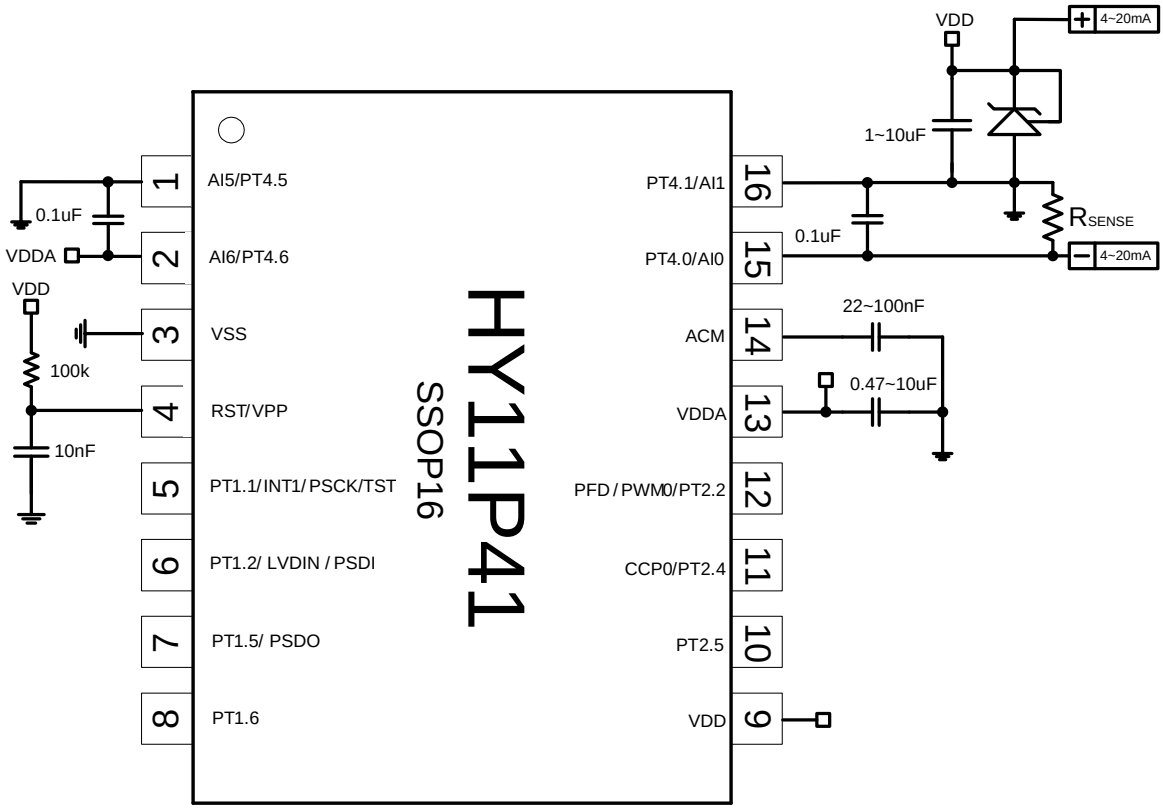


圖 3-3 無須外接電源的 4-20mA 表頭

註 1：關於零點電壓位置可透過 DCSET[2:0]進行偏壓調整

註 2：校正參數儲存可使用 BIE 功能取代之

4. 功能概述

4.1. 內部方塊圖

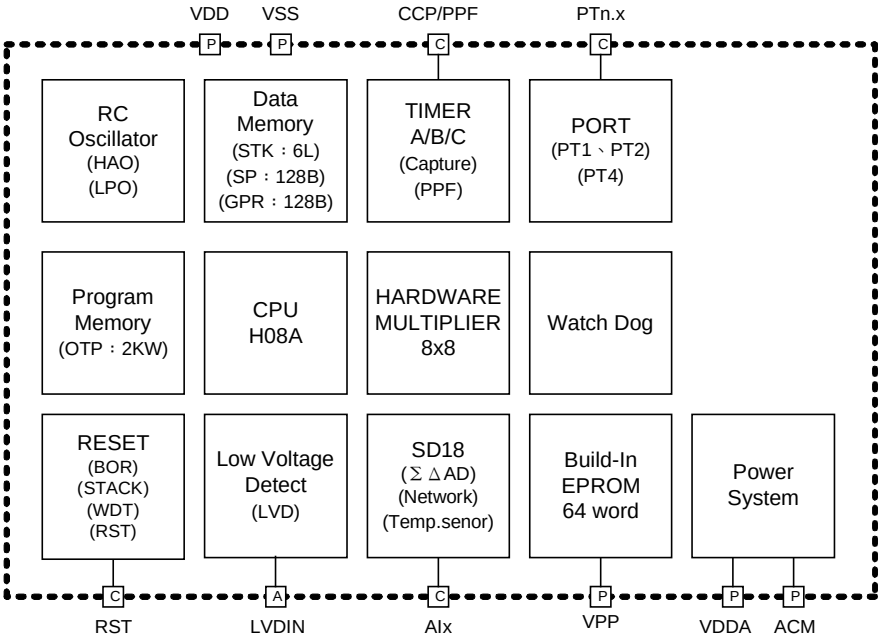


圖 4-1 HY11P41 內部方塊圖

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY11P41	HY11P41 說明書
UG-HY11S14	HY11Pxx 系列使用說明書
APD-CORE002-Vxx	H08A 指令說明書

開發工具相關使用說明書

APD-HYIDE006-Vxx	HY11xxx 系列開發工具軟體使用說明書
APD-HYIDE005-Vxx	HY11xxx 系列開發工具硬體使用說明書
APD-OTP001-Vxx	OTP 產品燒錄引腳說明書

產品生產相關使用說明書

APD-HYIDE004-Vxx	HY1xxxx 系列生產線專用燒錄器說明書
BDI-HY11P41-Vxx	HY11P41 個別產品的裸片打線資訊

4.3. SD18 Network

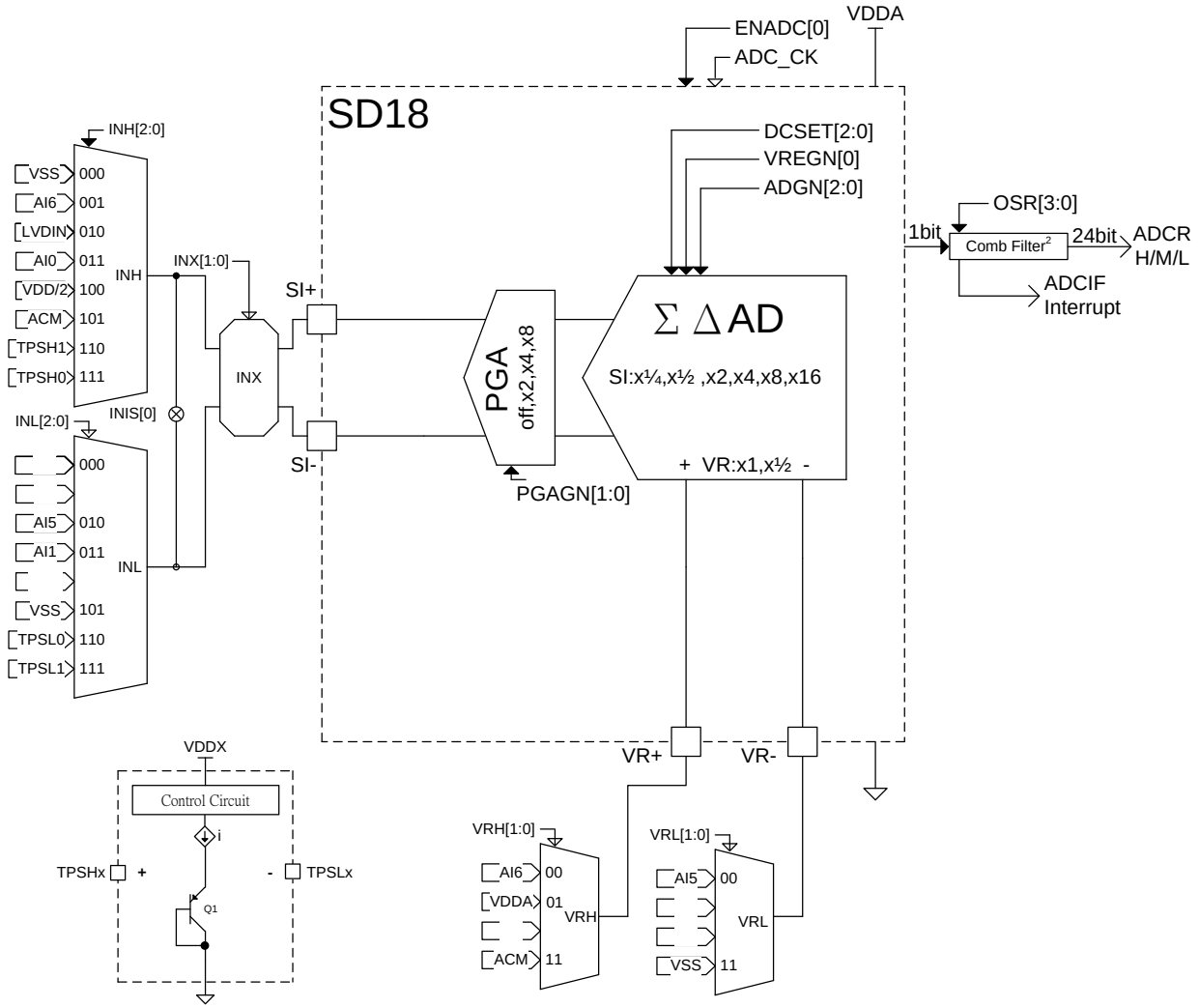


圖 4-2 SD18 Network

註 1：若 ADC 參考電壓端使用 AI6-AI5 網路連接到外部 VDDA-VSS 電源端，可以得到更高穩定度。

註 2：當使用開發工具(HY11S14-DK02)進行晶片模擬時，使用者需外接 AI8 類比網路到 VDDA 電源，用以達到 VRH[1:0]=01b 設定時，VRH 輸入為 VDDA 電壓源。外接 AI2 類比網路到 VSS 電源，用以達到 INH[2:0]=000b 設定時，INH 輸入為 VSS 電壓源。外接 AI4 類比網路到 PT1.2 引腳(LVDIN)，用以達到 INH[2:0]=010b 設定時，INH 輸入為 LVDIN 輸入源。

註 3：使用者也可以使用所提供 HY11P41 AD Net Board(PCB NO:T10009-2)連接到開發工具(HY11S14-DK02)類比輸入網路埠(Analog Port:JP3)，即可達成 AI8 與 AI2 類比網路電源設定。

5. 暫存器列表

“-”no use,“*”read/write,“w”write,“r”read,“r0”only read 0,“r1”only read 1,“w0”only write 0,“w1”omly write 1												
“.”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition												
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**i-RESET**	**R/W**
00H	INDF0	Contents of FSR0 to address data memory -value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
01H	POINC0	Contents of FSR0 to address data memory -value of FSR0 post-incremented								N/A	N/A	*,*,*,*,*,*,*,*
02H	PODEC0	Contents of FSR0 to address data memory -value of FSR0 post-decremented								N/A	N/A	*,*,*,*,*,*,*,*
03H	PRINC0	Contents of FSR0 to address data memory -value of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
04H	PLUSW0	Contents of FSR0 to address data memory -value of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
05H	INDF1	Contents of FSR1 to address data memory -value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
06H	POINC1	Contents of FSR1 to address data memory -value of FSR0 post-incremented								N/A	N/A	*,*,*,*,*,*,*,*
07H	PODEC1	Contents of FSR1 to address data memory -value of FSR0 post-decremented								N/A	N/A	*,*,*,*,*,*,*,*
08H	PRINC1	Contents of FSR1 to address data memory -value of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
09H	PLUSW1	Contents of FSR1 to address data memory -value of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
0FH	FSR0H								FSR0[8]	x	....u	-,-,-,- -,-,-,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
11H	FSR1H								FSR1[8]	x	....u	-,-,-,- -,-,-,*
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
16H	TOSH						TOS[10]	TOS[9]	TOS[8]	.... .000	.... .000	-,-,-,- -,*,*,*
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV			STKPRT[2:0]			000. .000	000. .000	r,rw0,rw0,- -,r,r,r
1AH	PCLATH						PC[10]	PC[9]	PC[8]	.... .000	.... .000	-,-,-,- -,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1DH	TBLPTRH						TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	.... .000	.... .000	-,-,-,- -,*,*,*
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1FH	TBLDH	Program Memory Table Latch High Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
21H	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
22H	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
23H	INTE1	GIE	ADCIE	TMCIE	TMBIE	TMAIE	WDTIE	E1IE		0000 000.	000. 000.	*,*,*,*,*,*,-
24H	INTE2						SSPIE		CCP0IE	.... .0.0	.... .0.0	-,-,-,- -,*,-,*
26H	INTF1		ADCIF	TMCIF	TMBIF	TMAIF	WDTIF	E1IF		.000 000.	.00. 000.	-,*,*,*,*,*,-
27H	INTF2						SSPIF		CCP0IF	.... .0.0	.... .0.0	-,-,-,- -,*,-,*
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
2AH	BSRCN								BSR[0]	0	0	-,-,-,- -,-,-,*
2BH	STATUS				C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
2CH	PSTATUS	PD	TO	IDLEB	BOR		SKERR			000d .0..	uduu .d..	rw0,rw0,rw0,rw0 -,rw0,-,-
2DH	LVDCN		LVDFG	LVD	LVDON	VLDX[3:0]				.000 0000	.000 uuuu	-,*,r,r *,*,*,*
30H	PWRCN	ENVDDA	VDDAX[1:0]		ENACM					0000	0000	*,*,*,* -,-,-,-
31H	MCKCN1	ADCS[2:0]			ADCCK				ENHAO	0000 ...1	0000 ...1	*,*,*,* -,-,-,*
32H	MCKCN2					HSS[1:0]		CPUCK[1:0]		 0000	 0000	-,-,-,- *,*,*,*
33H	MCKCN3					PERCK				.... 0...	.... 0...	-,-,-,- *,-,-,-
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3CH	ADCCN1	ENADC	ENHIGN	ENCHP	PGAGN[1:0]		ADGN[2:0]			0000 0000	0000 0000	*,*,*,*,*,*,*,*
3DH	ADCCN2					VREGN	DCSET[2:0]			 0000	 0000	-,-,-,- *,*,*,*
3EH	ADCCN3	OSR[2:0]						OSR[3]		000. ..0.	000. ..0.	*,*,*,- -,-,*,-
3FH	AINET1	INH[2:0]			INL[2:0]			INIS		0000 000.	0000 000.	*,*,*,*,*,*,-
40H	AINET2		VRH[1:0]		INX[1:0]		VRL[1:0]			.000 000.	.000 000.	-,*,*,*,*,*,-
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,* w1,*,*,*
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
43H	TMBCN	ENTMB	TMBCK	TMBS[1:0]		TMBSYC	TMBR2R			0000 00..	0000 00..	*,*,*,*,*,-
44H	TMBRH	TimerB High Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
45H	TMBRL	TimerB Low Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
46H	TMCCN	ENTMC	TMCCK[1:0]		TMCS1[2:0]			TMCS0[1:0]		0000 0000	0000 0000	*,*,*,*,*,*,*,*
47H	PRC	TimerC programmable register								1111 1111	1111 1111	*,*,*,*,*,*,*,*
48H	TMCR	TimerC register								0000 0000	0000 0000	r,r,r,r r,r,r,r
49H	CCPCN					CCP0M[3:0]				 0000	 0000	-,-,-,- *,*,*,*
4AH	CCP0RH	CCP0 High Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4BH	CCP0RL	CCP0 Low Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4FH	PWMCN	ENPWM	ENPFD	PWMRL[1:0]						0000	0000	*,*,*,* -,-,-,-
51H	PWMR	PWM MSB Byte register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
6AH	PT4		PT4.6	PT4.5				PT4.1	PT4.0	.xx. ..xx	.uu. ..uu	-,r,r,- -,-,r,r
6BH	PT4DA		DA4.6	DA4.5				DA4.1	DA4.0	.11. ..11	.11. ..11	-,*,*,- -,-,*,*
6CH	PT4PU		PU4.6	PU4.5				PU4.1	PU4.0	.00. ..00	.00. ..00	-,*,*,- -,-,*,*
6DH	PT1		PT1.6	PT1.5			PT1.2	PT1.1		.xx. .xx.	.uu. .uu.	-,*,*,- -,r,r,-
6EH	TRISC1		TC1.6	TC1.5						.00.	.00.	-,*,*,- -,-,-,-
6FH	PT1DA						DA1.2			.... .0..	.... .0..	-,-,-,- -,*,-,-
70H	PT1PU		PU1.6	PU1.5			PU1.2	PU1.1		.00. .00.	.00. .00.	-,*,*,- -,*,*,-
71H	PT1M1					INTEG1[1:0]				.... 00..	.... 00..	-,-,-,- *,*,-,-
72H	PT1M2				PM1.6[0]		PM1.5[0]			...0 .0..	...0 .0..	-,-,-,* -,*,-,-
74H	PT2			PT2.5	PT2.4		PT2.2			..xx .x..	..uu .u..	-,-,*,* -,*,-,-
75H	TRISC2			TC2.5	TC2.4		TC2.2			..00 .0..	..00 .0..	-,-,*,* -,*,-,-
77H	PT2PU			PU2.5	PU2.4		PU2.2			..00 .0..	..00 .0..	-,-,*,* -,*,-,-
78H	PT2M1			PM2.2[1]	PM2.2[0]					..00	..00	-,-,*,* -,-,-,-

表 5-1 HY11P41 暫存器列表

6. 電氣特性

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . . −0.2 V to 4.0 V

Voltage applied to any pin . . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . . −0.2 V to 6.9 V

Voltage applied to TST/PT1.1 pin . . . . . −0.2 V to V_{DD} + 1 V

Diode current at any device terminal . . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 150℃

(programmed device) . . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT2 I/O pin. 25mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage	All digital peripherals and CPU	2.2		3.6	V
		Analog peripherals	2.4		3.6	
V_{SS}	Supply Voltage		0		0	

6.2. Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.8	2.0	2.2	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

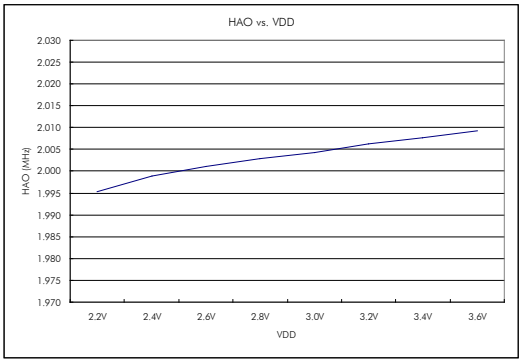


Figure 6.2-1 HAO vs. VDD

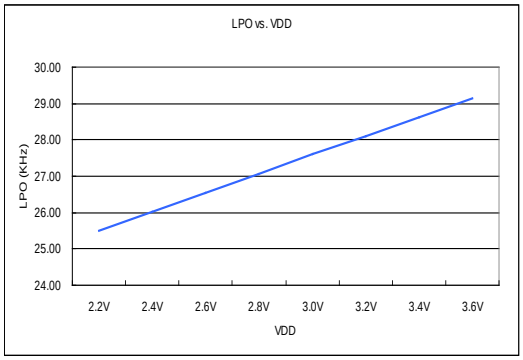


Figure 6.2-2 LPO vs. VDD

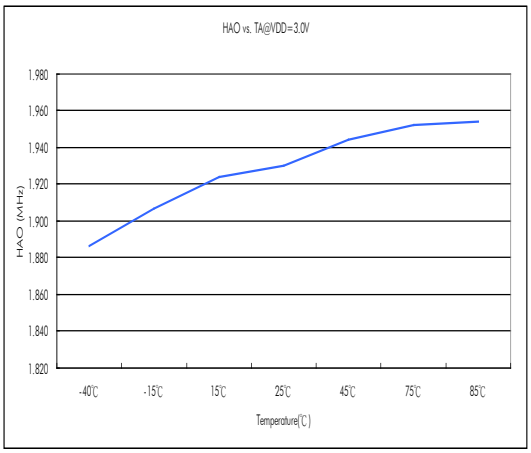


Figure 6.2-3 HAO vs. Temperature

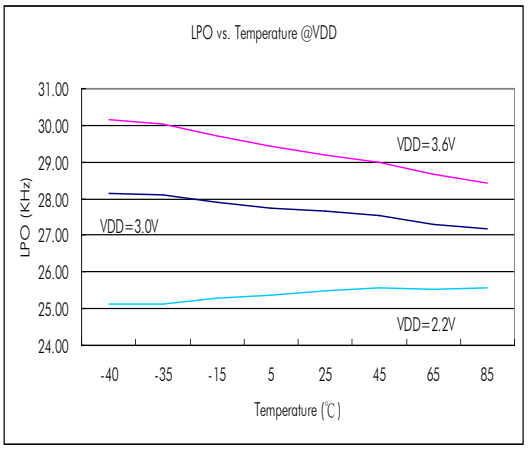


Figure 6.2-4 LPO vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 28KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM2}	Active mode 2	OSC_HAO = 2MHz, CPU_CK = 2MHz		0.32	0.55	mA
I_{AM3}	Active mode 3	OSC_HAO = 2MHz, CPU_CK = 1MHz		0.18	0.3	mA
I_{ILP2}	Low Power 2	OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

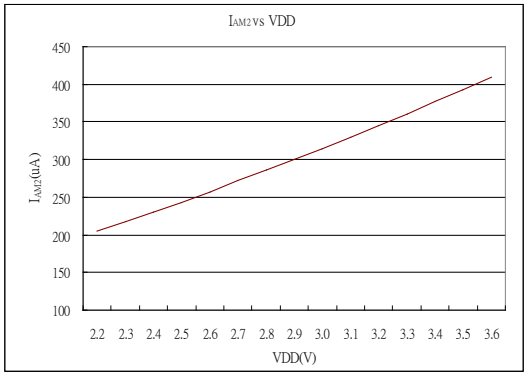


Figure 6.3-1 I_{AM2} vs. VDD

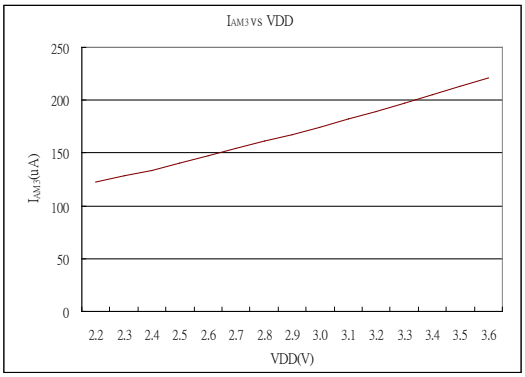


Figure 6.3-2 I_{AM3} vs. VDD

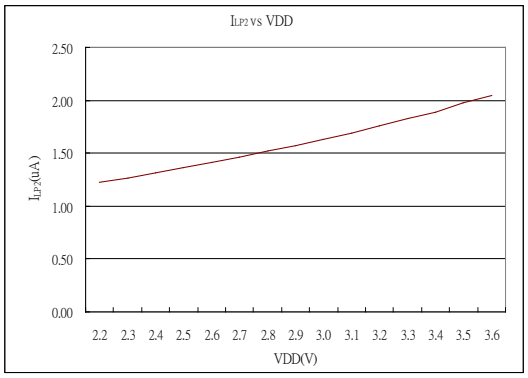


Figure 6.3-3 I_{LP2} vs. VDD

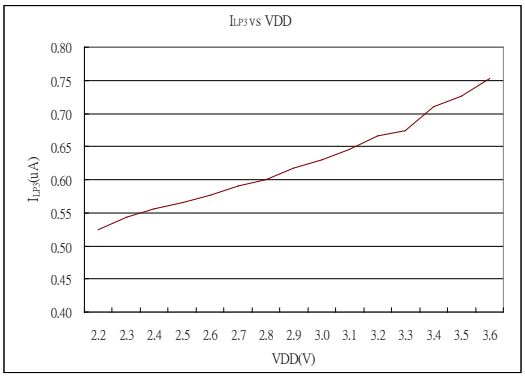


Figure 6.3-4 I_{LP3} vs. VDD

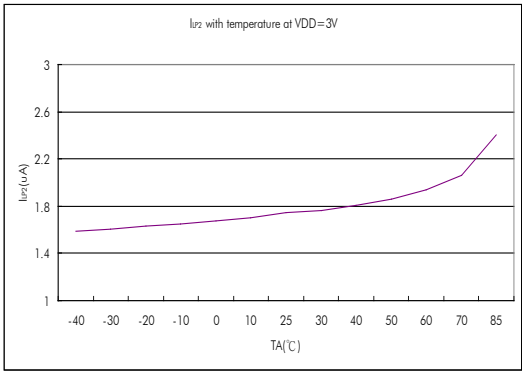


Figure 6.3-5 I_{LP2} vs. Temperature

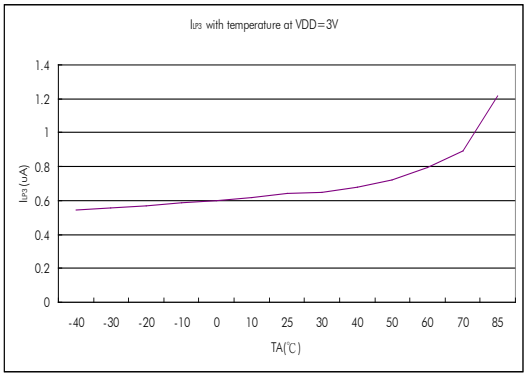


Figure 6.3-6 I_{LP3} vs. Temperature

6.4. Port1~4

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage		0.7*VDD		VDD	V
V_{IL}	Low-Level input voltage		VSS		0.3*VDD	
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

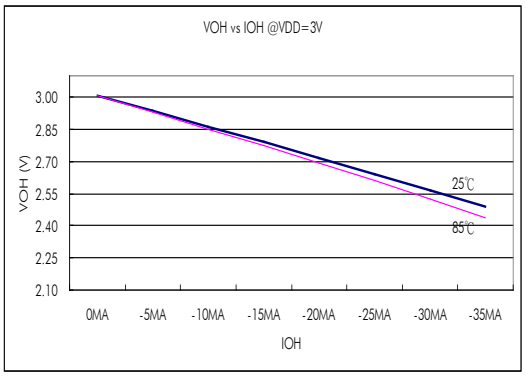


Figure 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V

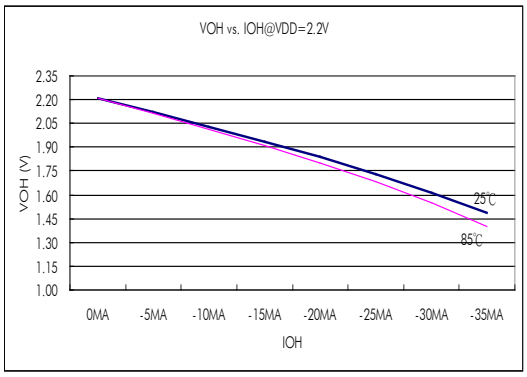


Figure 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V

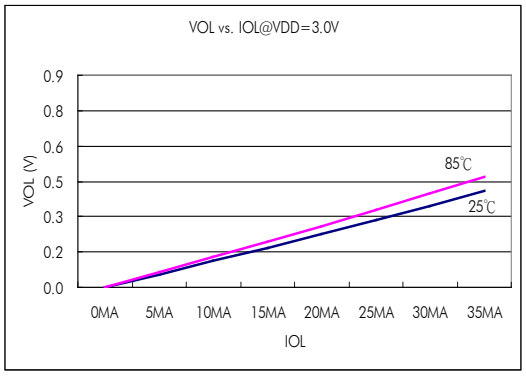


Figure 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V

Figure 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5. Reset(Brownout, External RST pin, Low Voltage Detect)

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V
LVD	Operation current, I_{SVS}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		100		ppm/℃
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

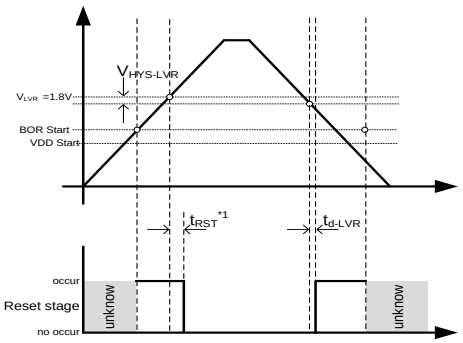


Figure6.5-1 BOR reset diagram

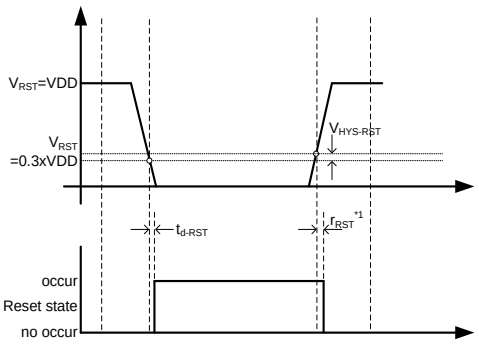


Figure6.5-2 RST reset diagram

*1 r_{RST} ：Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

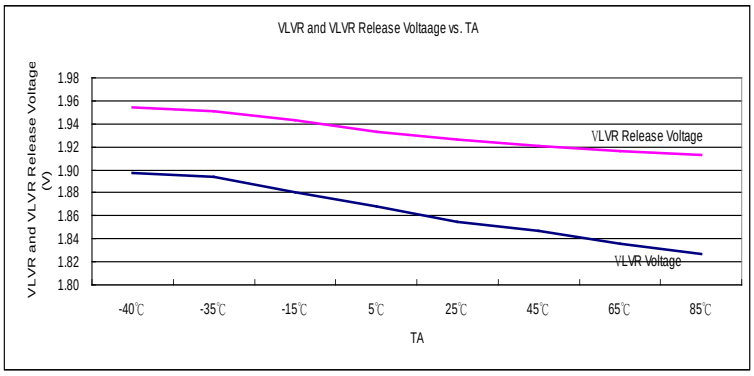


Figure6.5-3 LVR vs. Temperature

6.6. Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.2V	VDDAX[1:0]=00b		3.4		V
			VDDAX[1:0]=01b		3.0		V
			VDDAX[1:0]=10b		2.6		V
			VDDAX[1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX[1:0]=00b		135		mV
			VDDAX[1:0]=01b		150		mV
			VDDAX[1:0]=10b		165		mV
			VDDAX[1:0]=11b		180		mV
	Temperature drift	VDDAX[1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1, *1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Output voltage ,V_{ACM}	ENACM[0]=1, *2	I_L = 0uA		1.2		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1,	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift	I_L = 10uA			100		uV/V

VDDA：Adjust Voltage Regulator

ACM：Analog Common Mode Voltage

*1: V_{ACM} = 1.0V is just at A/D differential voltage reference < 1.4V (if delta VR: (VDDA-VSS)/2)

*2: V_{ACM} = 1.2V is just at A/D differential voltage reference > 1.4V (if delta VR: (VDDA-VSS)/2)

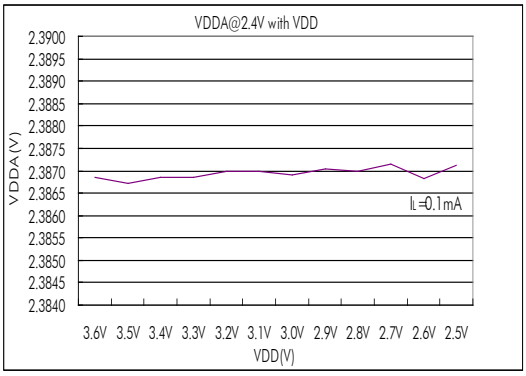


Figure6.6-1 VDDA I_L=0.1mA vs. VDD

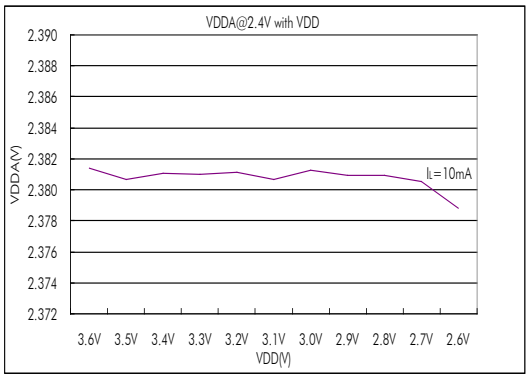


Figure6.6-2 VDDA I_L=10mA vs. VDD

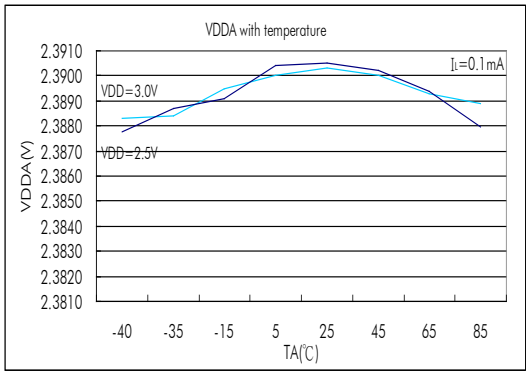


Figure6.6-3 VDDA I_L=0.1mA vs. Temperature

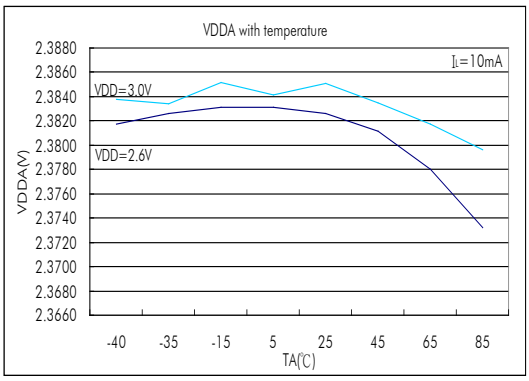


Figure6.6-4 VDDA I_L=10mA vs. Temperature

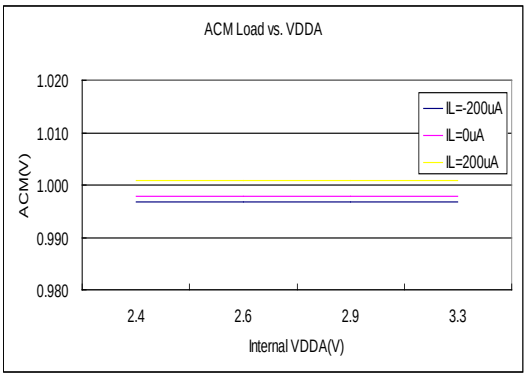


Figure6.6-5 ACM Load vs. VDDA (a)

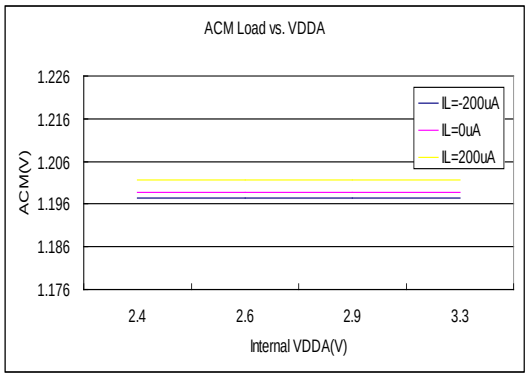


Figure6.6-5 ACM Load vs. VDDA (b)

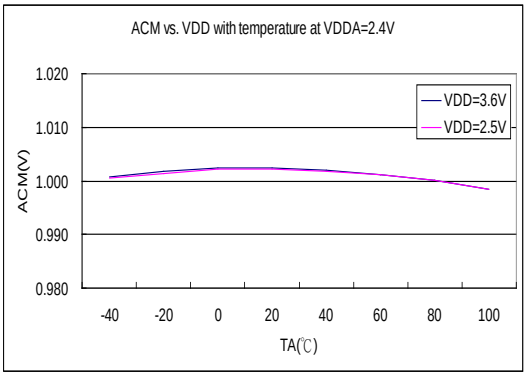


Figure6.6-6 ACM vs. Temperature (a)

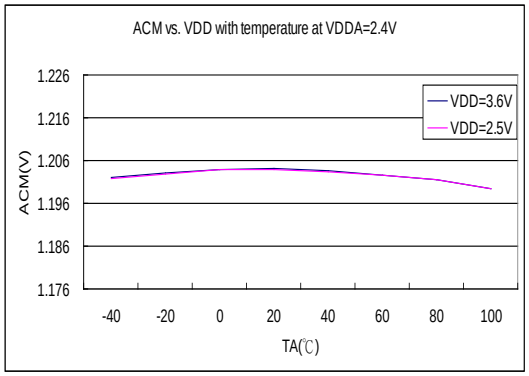


Figure6.6-6 ACM vs. Temperature (b)

6.7. SD18,Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			128 *1		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1	GAIN =4, ADC_CK=250KHz		120		uA
*1, OSR=128, setting by ADCCN3[OSR[3]] bit. OSR[3:0]=1010, OSR=128; OSR[3:0]=0xxx, OSR=256 ~ 32768							

6.7.1. PGA, Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<01>or<1x>			320		uA
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=128		5		ppm/℃

6.7.2. SD18,performance Ⅱ (fSD18=250KHz)

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV			±0.003	±0.01	%FSR
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b		23			Bits
G_{SD18}	Temperature drift **Gain 1~x16**		T_A= -40℃~ 85℃		2		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short	Gain=2			1	%FSR
	Offset temperature drift with chopper without PGA		GAIN=1		2		uV/℃
			GAIN=2		1		
			GAIN=4		0.5		
			GAIN=16		0.15		
			GAIN=128		0.02		

CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1	90	dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,	V_{SI}=0V, GAIN=16	75	
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV, V_{VR}=1.0V, V_{SI}=V_{SI-}=1.2V,	GAIN=1 PGA=off	75	dB
			GAIN=16		

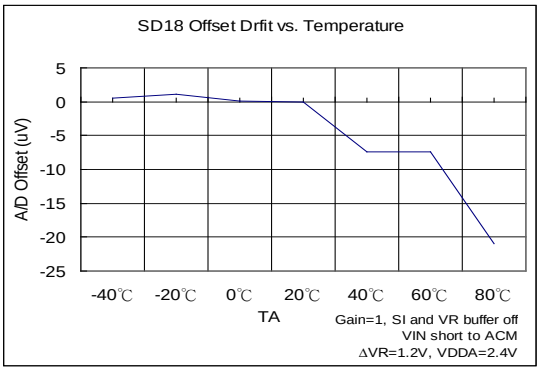


Figure6.7-1(a) SD18 Offset Temperature drift

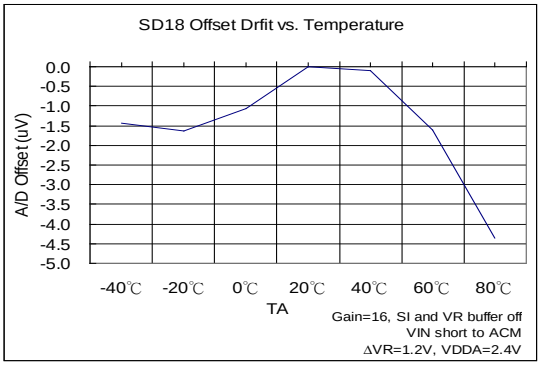


Figure6.7-1(b) SD18 Offset Temperature drift

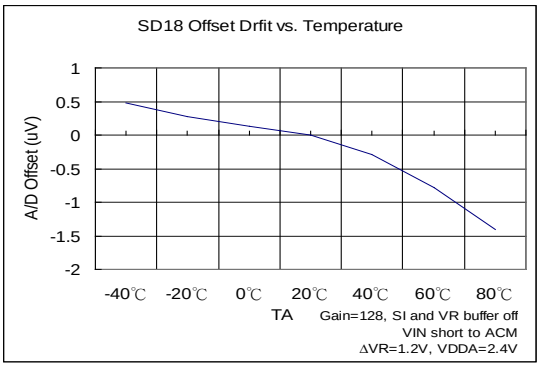


Figure6.7-1(c) SD18 Offset Temperature drift

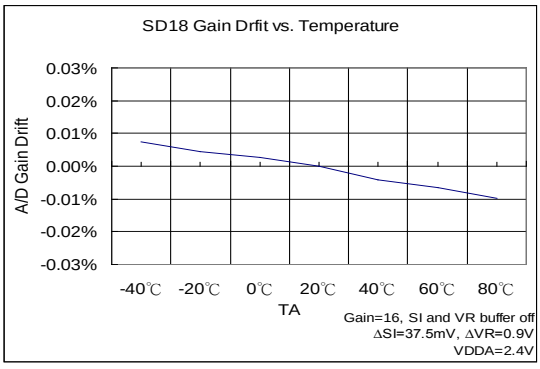


Figure6.7-2(b) SD18 Gain drift with temperature

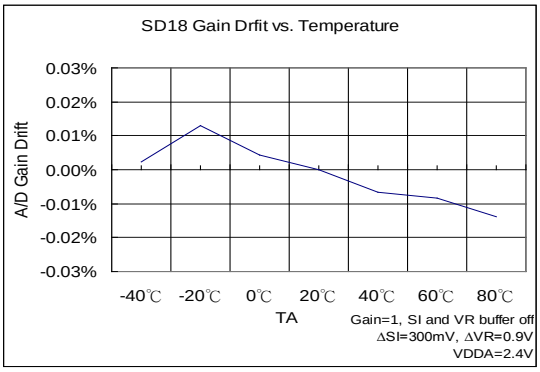


Figure6.7-2(a) SD18 Gain drift with temperature

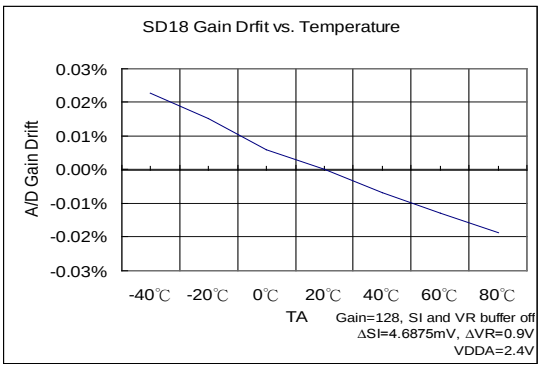


Figure6.7-2(c) SD18 Gain drift with temperature

6.7.3. SD18,Temperature sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			178		uV/℃
KT	Absolute Temperature Scale 0°K			-289		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~ 85℃		±2		℃

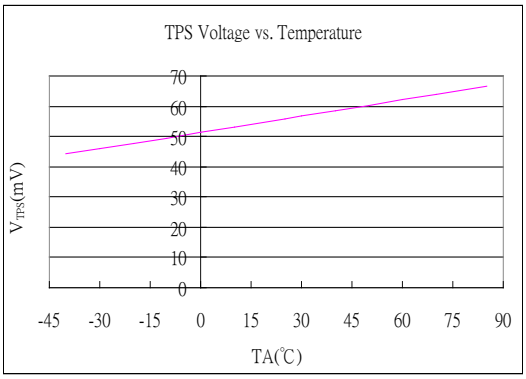


Figure6.7-3 TPS output voltage vs. temperature drift

6.7.4. SD18 Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY11P41 針對 SD18 提供了重要的輸入雜訊規格。Table6.7-4(a), Table6.7-4(b) 列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在外部輸入訊號短路，ADC 參考電壓源為使用外部 VDDA 及外部 VSS 當參考電壓源網路，等效參考電壓為 1.2V，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V														
Max. Vin(mV) =0.9*VREF (1)	OSR					128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					1953	977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN									
±2400	0.25	=	1	×	0.25	14.0	16.3	17.6	18.3	18.9	19.4	19.8	20.3	20.7
±2160	0.5	=	1	×	0.5	13.9	16.2	17.5	18.2	18.8	19.3	19.7	20.2	20.6
±1080	1	=	1	×	1	14.0	16.2	17.4	18.1	18.6	19.1	19.5	19.9	20.4
±540	2	=	1	×	2	13.9	16.1	17.3	17.9	18.4	18.9	19.4	19.8	20.2
±270	4	=	1	×	4	13.9	16.0	17.0	17.7	18.1	18.6	19.1	19.6	20.0
±135	8	=	1	×	8	13.9	15.9	16.7	17.3	17.8	18.2	18.8	19.2	19.7
±68	16	=	1	×	16	13.8	15.6	16.3	16.8	17.3	17.8	18.3	18.8	19.3
±34	32	=	2	×	16	13.5	14.8	15.4	15.9	16.4	16.9	17.4	17.9	18.4
±17	64	=	4	×	16	13.4	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.1
±8	128	=	8	×	16	13.1	14.1	14.6	15.1	15.6	16.1	16.6	17.1	17.6

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table6.7-4(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V														
Max. Vin(mV) =0.9*VREF	OSR					128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					1953	977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN									
±2400	0.25	=	1	×	0.25	680.48	122.16	47.79	29.08	20.02	14.45	10.35	7.55	5.90
±2160	0.5	=	1	×	0.5	355.63	63.41	25.72	15.67	10.78	7.66	5.63	3.99	2.97
±1080	1	=	1	×	1	166.02	31.71	13.93	8.63	5.99	4.35	3.22	2.41	1.76
±540	2	=	1	×	2	85.85	16.80	7.72	4.96	3.49	2.49	1.81	1.33	0.98
±270	4	=	1	×	4	43.52	9.19	4.53	2.93	2.12	1.51	1.08	0.78	0.59
±135	8	=	1	×	8	22.18	5.10	2.83	1.91	1.33	0.97	0.67	0.49	0.35
±68	16	=	1	×	16	11.97	3.08	1.88	1.30	0.91	0.66	0.46	0.33	0.23
±34	32	=	2	×	16	6.75	2.63	1.79	1.24	0.87	0.62	0.44	0.32	0.22
±17	64	=	4	×	16	3.75	1.68	1.12	0.80	0.56	0.42	0.28	0.20	0.14
±8	128	=	8	×	16	2.16	1.09	0.78	0.55	0.38	0.27	0.19	0.13	0.10

Table6.7-4(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024}(\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

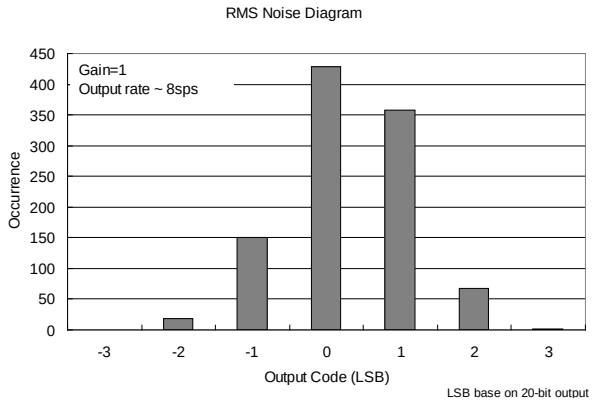


Figure6.7-4(a) RMS Noise Diagram

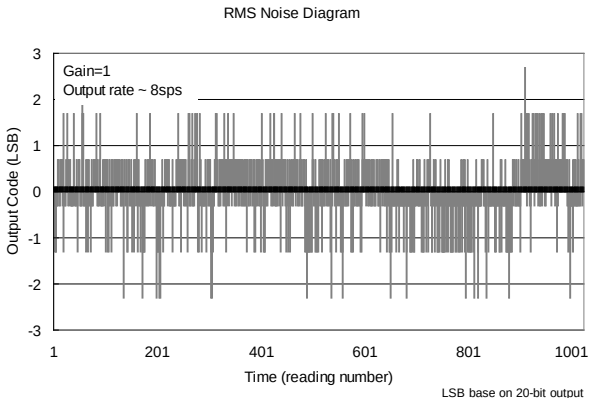


Figure6.7-4(b) Output Code Diagram

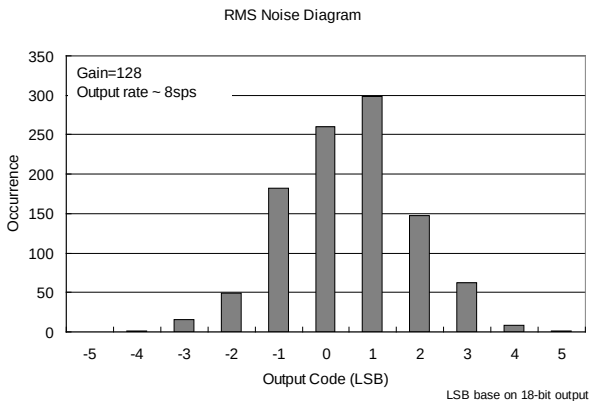


Figure6.7-4(c) RMS Noise Diagram

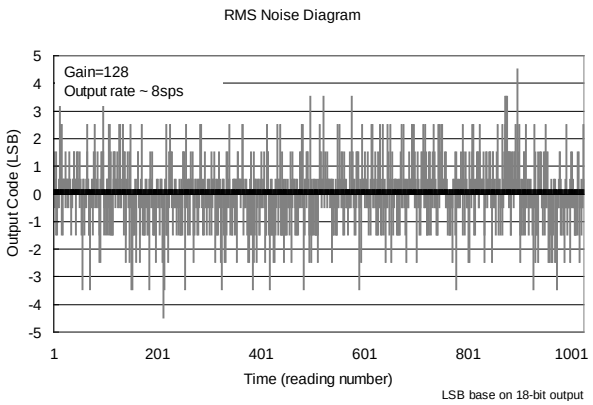


Figure6.7-4(d) Output Code Diagram

6.8. Build-In EPROM(BIE)

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage			6.0	6.5	V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V

7. 訂貨資訊

下單品名[1]	封裝型式	引腳數	封裝型式描述方式		程式碼編號[2]	出貨包裝形式	個裝數量	材料組成	MSL[3]
HY11P41-D000	Die	-	D	000	000	-	250	Green[4]	-
HY11P41-E016	SSOP	16	E	016	000	Tube	100	Green[4]	MSL-3
HY11P41-E016	SSOP	16	E	016	000	Tape & Reel	2500	Green[4]	MSL-3
HY11P41-S016	SOP	16	S	016	000	Tube	50	Green[4]	MSL-3
HY11P41-S016	SOP	16	S	016	000	Tape & Reel	2500	Green[4]	MSL-3
HY11P41-N016	QFN	16	N	016	000	Tape & Reel	5000	Green[4]	MSL-3

[1] 產品名稱 – 封裝型式描述方式 – 程式碼編號（空白片 / 標準品 / 代客燒錄碼）

例如：您的代客燒錄服務申請的程式碼編號為 008，且需要的產品是裸片出貨。則下單品名為 HY11P41-D000-008

例如：您的需求是不帶程式碼的空白片且需要的產品是裸片出貨。則下單品名為 HY11P41-D000

例如：您的需求是不帶程式碼的空白片且需要的產品是封裝片 SSOP16 出貨，則下單品名為 HY11P41-E016，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 SOP16 出貨，則下單品名為 HY11P41-S016-009，且需以 Tube 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tube

[2] 程式碼編號

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] **MSL**

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

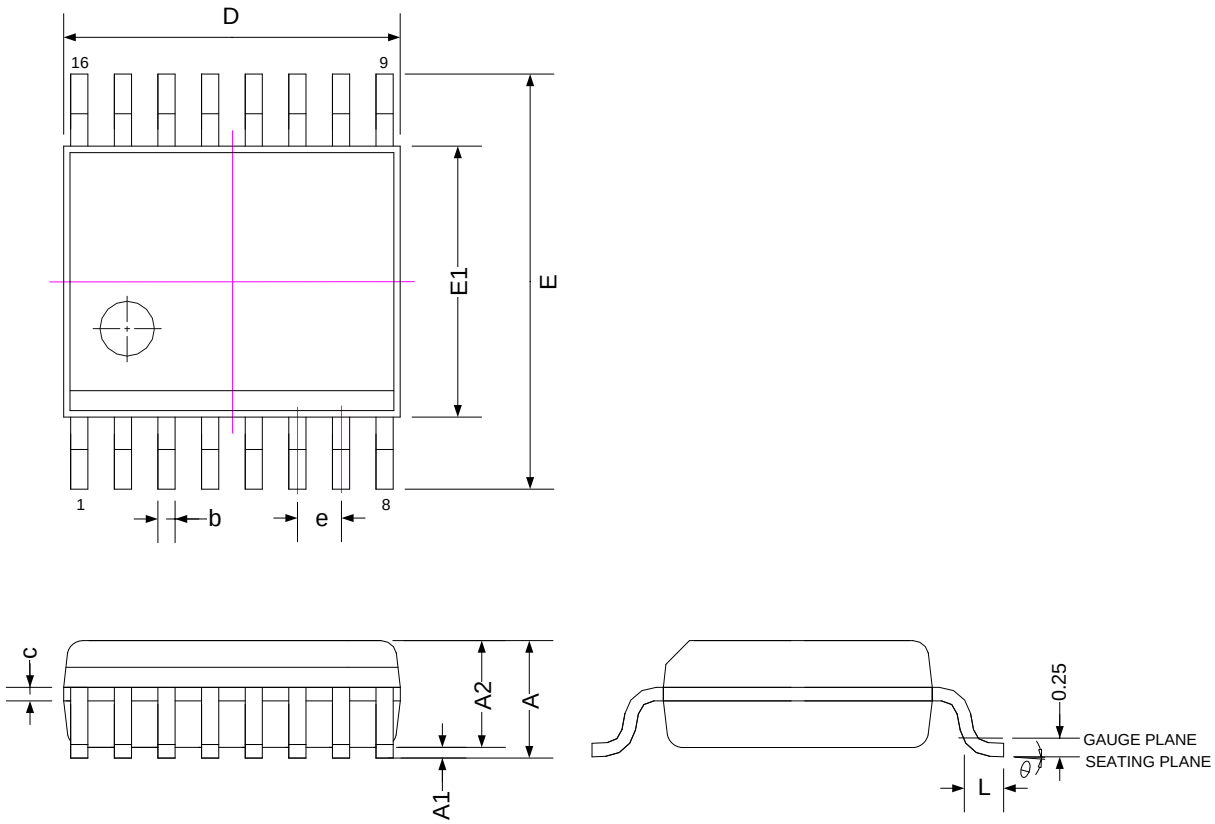
[4] **Green (RoHS & no Cl/Br)**

HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC)以及無鹵素相關規定。

8. 封裝型式資訊

8.1. SSOP16(E016)

8.1.1. Package Dimensions

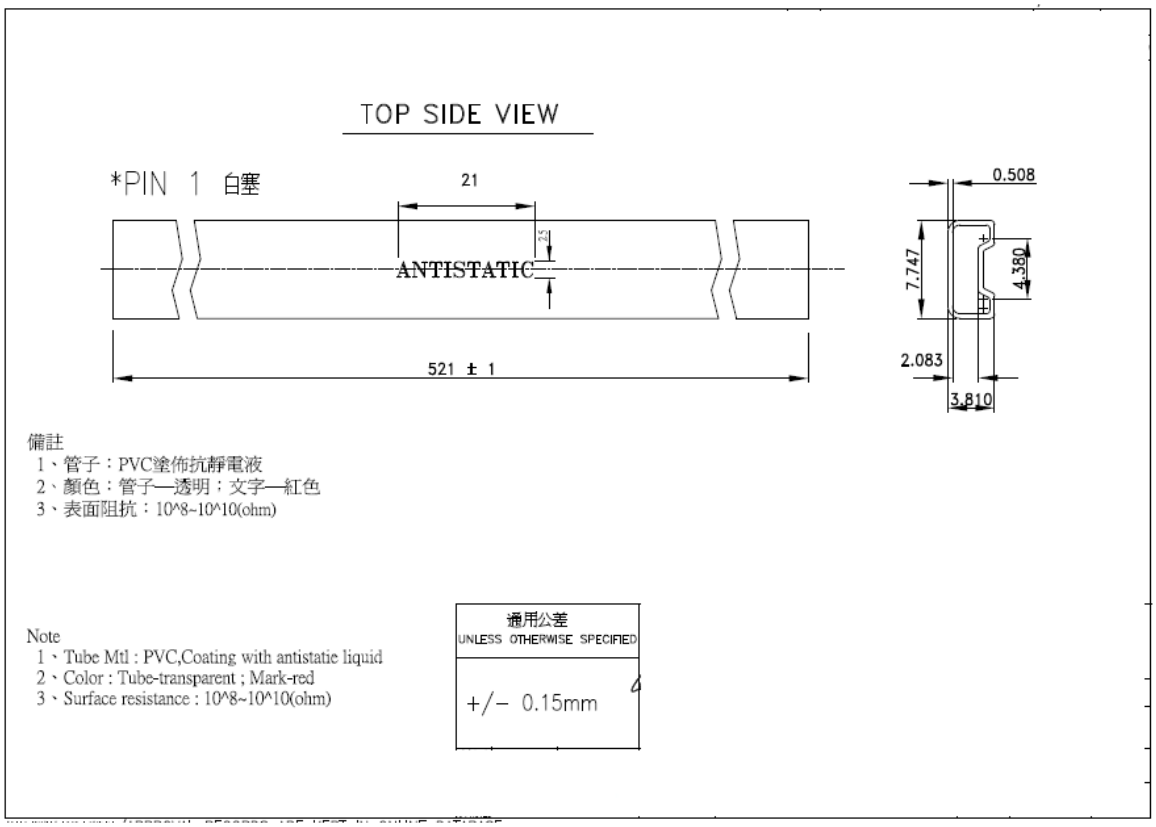


SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	4.80	4.90	5.00
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	-	1.27
e	0.635 BASIC		
θ°	0	-	8

Note：

1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit : mm.

8.1.2. Tube Dimensions



備註
1、管子：PVC塗佈抗靜電液
2、顏色：管子—透明；文字—紅色
3、表面阻抗：10^8~10^10(ohm)

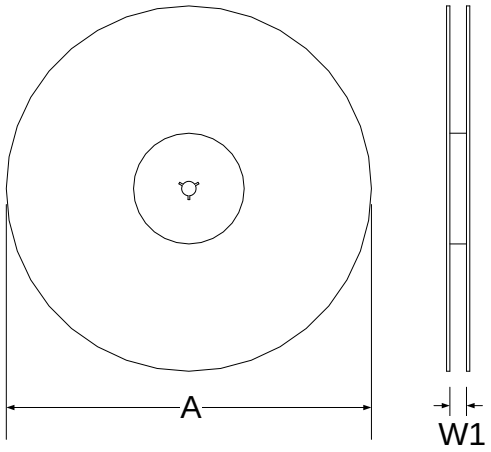
Note
1、Tube Mtl : PVC,Coating with antistatic liquid
2、Color : Tube-transparent ; Mark-red
3、Surface resistance : 10^8~10^10(ohm)

通用公差 UNLESS OTHERWISE SPECIFIED
+/− 0.15mm

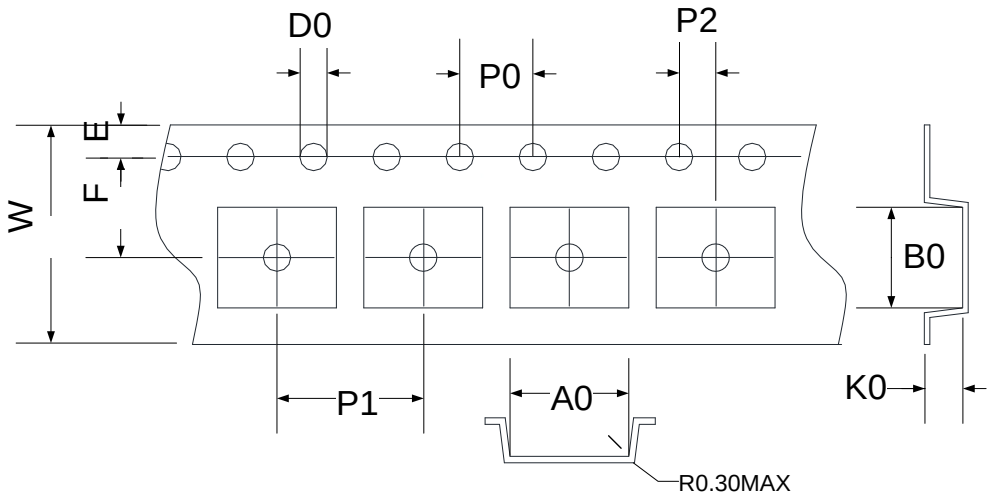
8.1.3. Tape & Reel Information

8.1.3.1. Reel Dimensions –Type1

Unit : mm

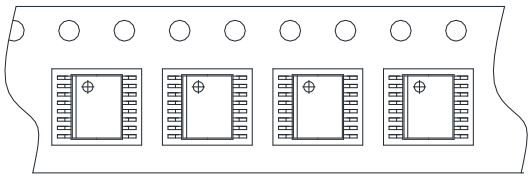


8.1.3.2. Carrier Tape Dimensions



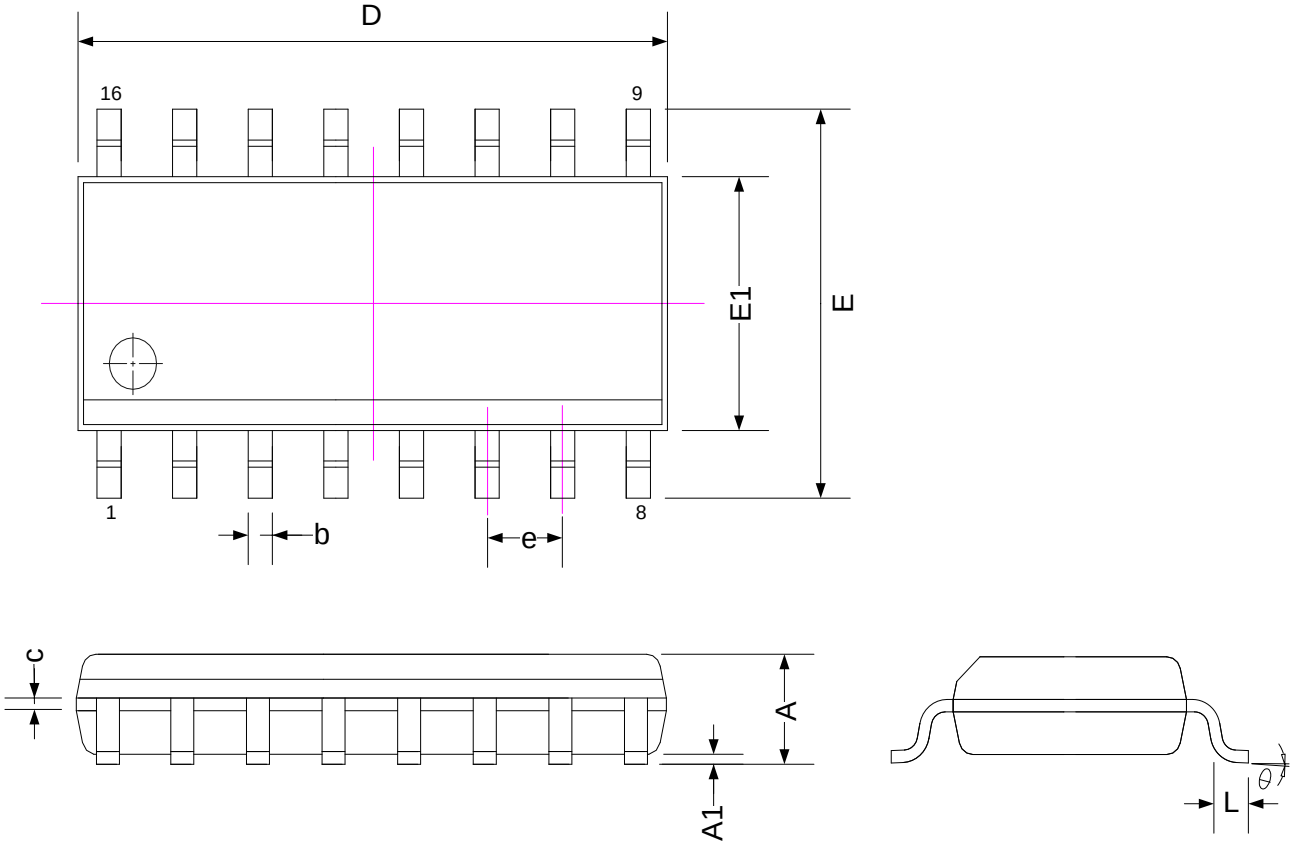
SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.90	5.40	2.00	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

8.1.3.3. Pin1 direction



8.2. SOP16(S016)

8.2.1. Package Dimensions

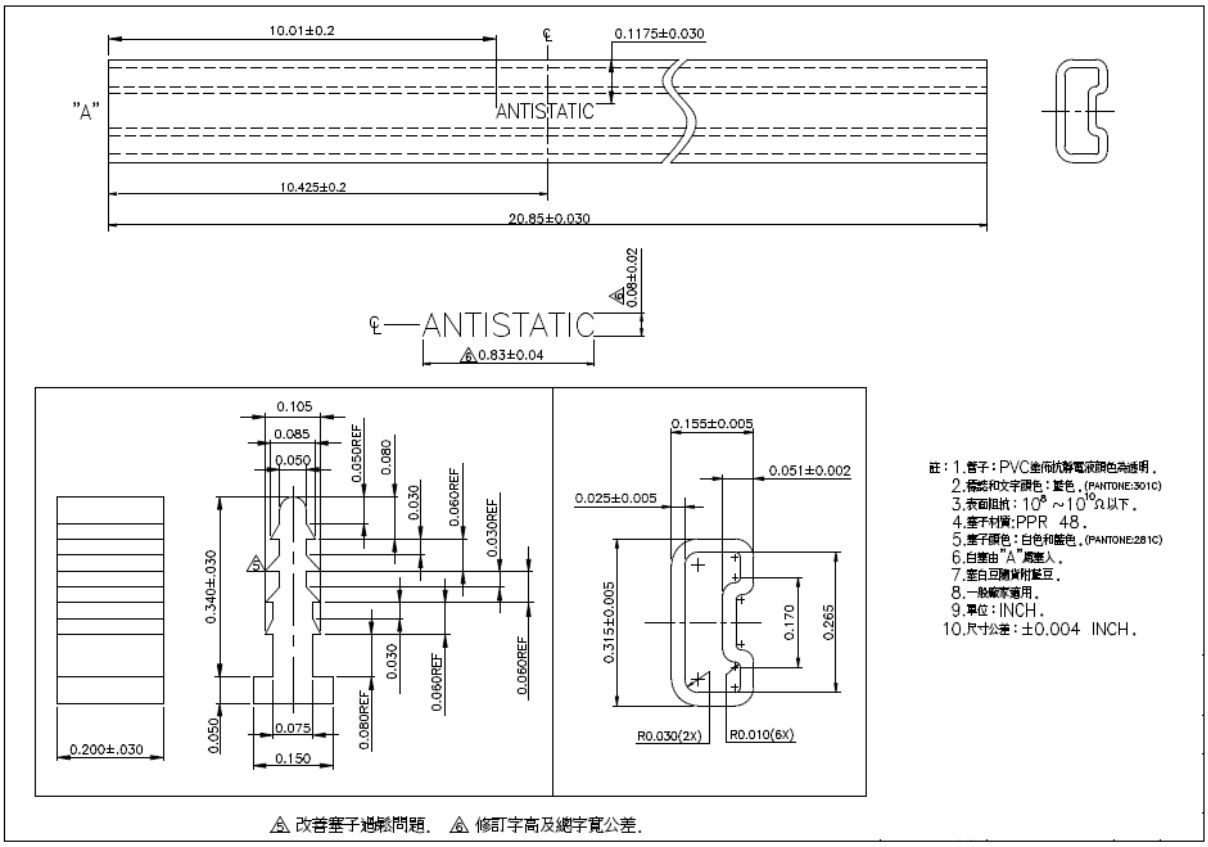


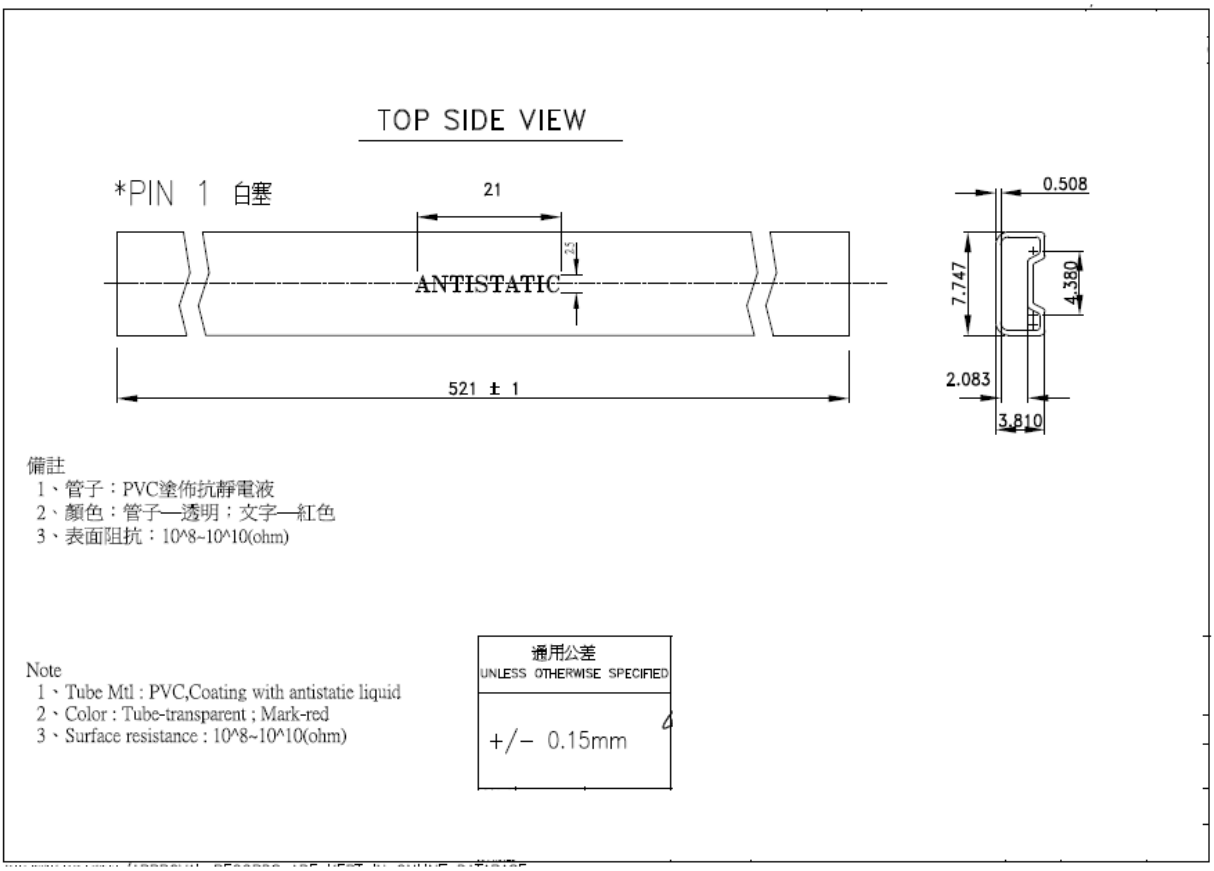
SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
b	0.31	-	0.51
c	0.10	-	0.25
D	9.90 BASIC		
E1	3.90 BASIC		
E	6.00 BASIC		
L	0.40	-	1.27
e	1.27 BASIC		
θ	0	-	8

Note：

1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2.2. Tube Dimensions

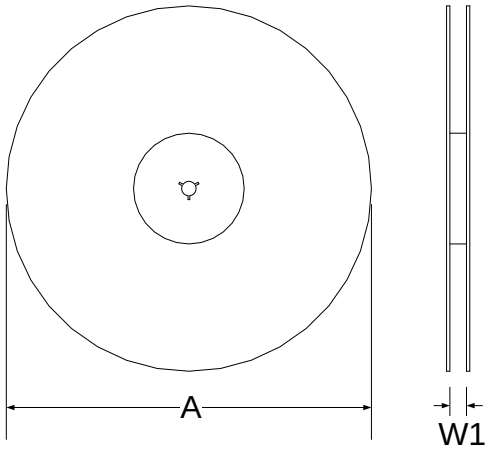




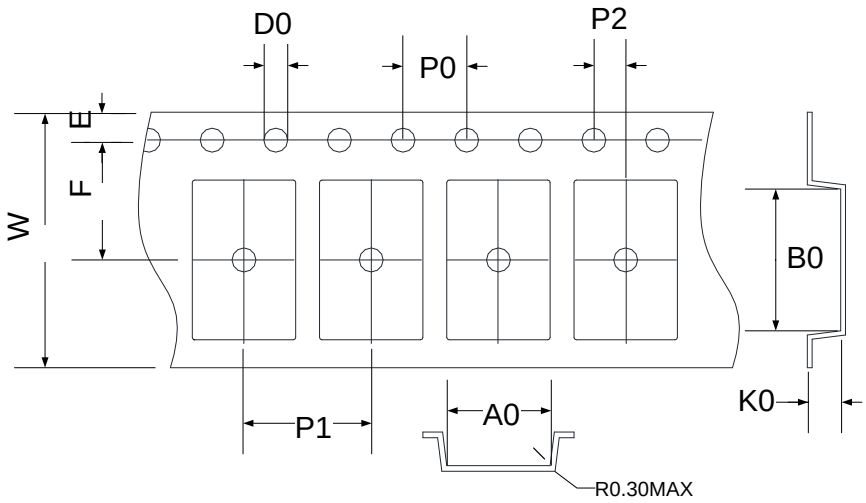
8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions –Type1

Unit : mm

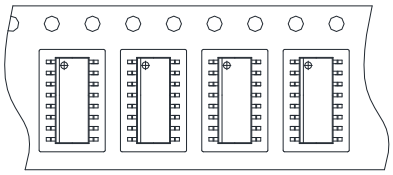


8.2.3.2. Carrier Tape Dimensions



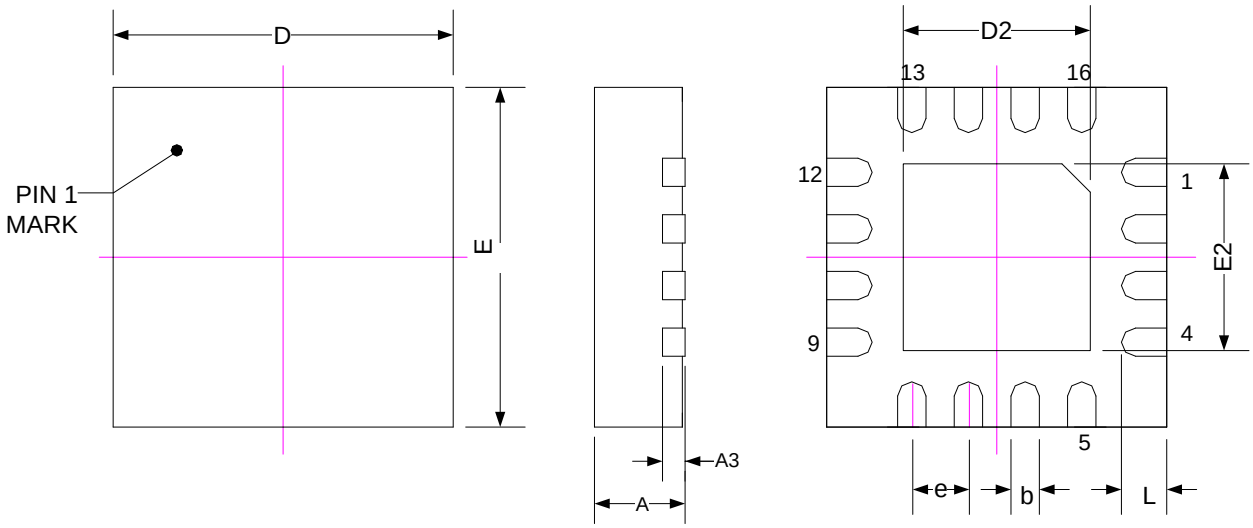
SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	10.30	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

8.2.3.3. Pin1 direction



8.3. QFN16(N016)

8.3.1. Package Dimensions

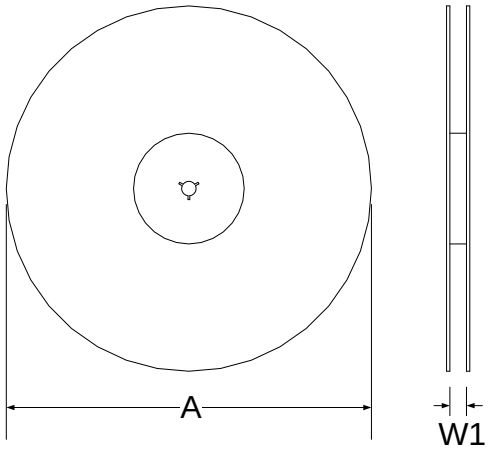


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A3		0.203 REF.	
b	0.20	0.25	0.30
D	2.925	3.000	3.075
E	2.925	3.000	3.075
D2	1.625	1.725	1.825
E2	1.625	1.725	1.825
L	0.30	0.35	0.40
e		0.50 BASIC	

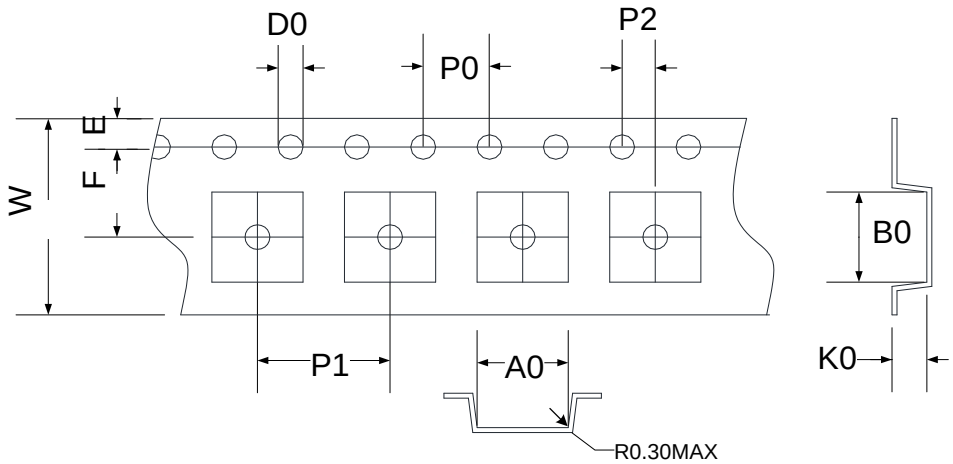
8.3.2. Tape & Reel Information

8.3.2.1. Reel Dimensions –Type1

Unit : mm

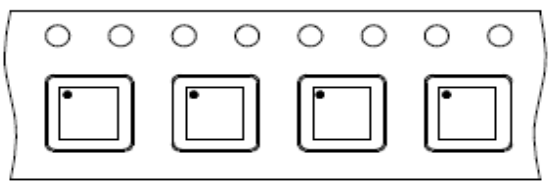


8.3.2.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	3.30	3.30	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

8.3.2.3. Pin1 direction



9. 修訂記錄

以下描述本檔差異較大的地方，而標點符號與字形的改變不在此描述範圍。

版本	頁次	變更摘要
V01	ALL	初版發行
V02	5~10	修改腳位名稱順序
	6	修改腳位名稱定義方式
	13	修改表 5-1 暫存器列表，刪除 PASC 暫存器
V03	4	修改特點內容
	5	增加 SOP16 引腳圖
	23	增加 OSR 說明
	26~27	修改 SD18 Noise Performance
	29	增加訂貨資訊
	31	增加封裝形式資料
V04	4	修改特點內容，刪除 COMPARE 功能
	6	修改 I/O 引腳定義內容
	11	修改內部方塊圖內容
	21	增加 Power System 內容說明
V05	12	修改圖 4-2 SD18 Network
	21	修改 Power System 規格內容
V06	11	修改開發工具相關使用說明書編號
	29	增加訂貨資訊內容
V07	12	增加 SD18 Network 說明
V08	All	增加 QFN16 封裝形式內容
V09	5	增加串列通訊 SPI 模組使用說明
V10	5~17,19	刪除串列通訊 SPI 模組相關說明
V11	5	增加快速功能啓動描述
	14~16	更新電路圖 VDDA 容值與增加 VDD 電容元件
	29	刪除 ADC INBF, ADC VRBF 描述
	36~37	更新封裝形式資訊 SSOP16,SOP16 表示方式
V12	6~16,20	修正 PT1.1/TST 引腳內容
V13	35	HY11P41-N016 訂貨資訊 (3000/Reel 修改為 5000/Reel)
V14	5	新增功能列表
	11~12	新增封裝型式與正印說明
	33	更新 Green(RoHS & no Cl/Br)
	36	新增 Tape & Reel Information

39	新增 Tape & Reel Information
41	新增 Tape & Reel Information