Thin Film Transfer by Smart Cut Technology beyond SOI

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During the last decade the substrate industry has brought the 8" substrate technology to maturity with the introduction of Nearly Perfect Crystal wafers, and two major innovations at the substrate level have occurred : the development of 300mm Silicon has been the response to the economy of scale of the 0.18µm IC technology node with a more aggressive introduction for technologies below 100nm; and SOI, Silicon on Insulator, has been the response to the IC requirements of improved performance while reducing the parasitic substrate capacitances and leakage currents.

The SOI substrates constitute without doubt a paradigm shift of the Silicon IC industry. The early SOI days as a niche substrate technology for military or space applications are long over. SIMOX, wafer bonding and grind back, the first SOI wafer manufacturing technologies, have also strongly improved during the past 10 years but the SOI boom arrived with the breakthrough made by Smart-Cut technology. Smart-Cut is a bonding and thin layer transfer technique from a donor wafer onto a handle substrate. The transferred layer thickness is pre-determined by the cleavage zone created via ion implantation (hydrogen, helium, argon, etc.). After the layer transfer, the cleaved surface of the thin film is treated, polished and annealed to ensure a Silicon film and surface quality comparable to Silicon prime wafers.

As the IC industry moves towards the development of the future 65nm, 45nm, 32nm technology nodes more innovations will be required at the substrate level. The IC industry will likely experience a similar shift as the one seen in the 90s with the development of IC process modules by the equipment manufacturers. Strained silicon is today one of the latest substrate developments as an answer to the manufacturing of very high performance devices. The manufacturing of these substrates require several Si and SiGe epitaxial steps to be able to obtain the strained silicon layer at the substrate surface. As a function of the level of the build-in strain in Si lattice an enhancement of the electron and hole mobility up to 50% can be achieved, which translates into an improved MOSFET performance. Strained Silicon bulk wafers are still far from meeting the specifications of state-of-the-art Si and SOI wafers but development continues at a very high pace.

Smart-Cut is the technology that enables the development of ultra thin strained Si on insulator which will be needed by the fully depleted MOSFET architecture of the 65nm IC technology node while reducing the overall cost-of-ownership of such high end substrates. The development of ultra-thin strained Si on insulator is underway in order to meet the future substrate needs of the IC industry towards more performing devices while keeping the power consumption at low levels. The strong synergy between the ultra-thin SOI (<500A Si thickness on oxide) and ultra-thin strained Si is one of the factors that makes possible the fast development of this new generation of 300mm wafers.

The potential wafer solutions offered by the Smart-Cut technology are already much greater than just SOI and strained Silicon on insulator. A current development is Silicon on Quartz (SOQ). It offers a single crystal Silicon layer on a fused quartz substrate, a development that will be extendable to Silicon on glass. Silicon on Quartz will enable the industry to couple for the first time the Si IC state-of-the-art know-how with transparent substrates.

The know-how acquired through the SOI development has opened another door, the engineering of the bonding energy to allow post processing debonding of the structure containing layer. The debonding technology of IC processed Silicon layers makes it possible to obtain Silicon films a 100 times thinner than the state-of-the-art wafer thinning techniques. Commonly fully processed IC wafers are lapped down to a thickness of 100 to 150µm, the smart card industry requires wafer thinning down to 40-50µm, the state-of-the-art today. With debondable Smart-Cut wafers, wafer scale processed Silicon films in the range of 0.2 to 1µm thickness can be obtained. The availability of this wafer technology will empower the IC industry with a wide range of totally new solutions and applications mainly in packaging, advanced very flexible smart-cards, 3D-SOC, etc. In order to reduce for example, the detrimental self heating effects in ICs, the utilization of heat conducting substrates will be necessary leading to a new generation of SOI wafers with a buried thermal sink.

The flexibility of the Smart-Cut technology has very interesting applications beyond the Silicon world in photonics, opto-electronics, high frequency and high power devices with the development of hetero-composite substrates.

As we move into the new 21st century we will see substrate manufacturers acquire more responsibility in the making of ICs through the development of more complex, partially processed substrates, tailored to specific applications. More visibility of the IC integration process will be needed to enable the wafer manufacturers to develop the suitable wafer solutions in a similar manner to the evolution seen among the equipment manufacturers in the 90s.