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AEC-Q100, Q101, Q200

Prisemi
Date: 2017/9/04

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Self-Introduction

Hanson Zheng (郑朝晖)

教育经历:

1991~1995	SJTU	学士 精密仪器专业
1995~1998	SJTU	硕士 电子工程测控

工作经历:

1998~2004	Beilling	测试工程经理
2004~2004	Amlogic	运营经理
2004~2011	Atheros	中国区运营总监
2011~2017	Qualcomm	工程总监
2017~Now	Prisemi	工程质量副总经理

車用電子零件分為三大類別，包含IC、離散半導體、被動元件三大類別，

AEC-Q100	IC集成电路
ACE-Q101	离散元器件
AEC-Q200	被动元件

為了確保這些汽車電子零組件符合汽車安全的最高標準，美國汽車電子協會(AEC，Automotive Electronics Council)係以主動零件[微控制器與積體電路..等]為標的所設計出的一套標準 [AEC-Q100]、針對被動元件設計為[[AEC-Q200]，其規範了被動零件所必須達成的產品品質與可靠度，AEC-Q100為AEC組織所制訂的車用可靠性測試標準，為3C&IC廠商打進國際車用大廠模組的重要入場卷。此外，目前國際大廠已經通過車用安全性標準(ISO-26262)，而AEC-Q100則為通過該標準的基本要求。

AEC規範免費下載網頁：
http://www.aecouncil.com/AECDocuments.html

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汽车电子零件工作溫度等級定義：

0等級：環境工作溫度範圍-40℃～150℃
1等級：環境工作溫度範圍-40℃～125℃
2等級：環境工作溫度範圍-40℃～105℃
3等級：環境工作溫度範圍-40℃～85℃
4等級：環境工作溫度範圍0℃～70℃

AEC 规范

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簡稱	中文	英文	說明
AEC	美國汽車電子協會	Automotive Electronic Council	由車廠[克萊斯勒(Chrysler)、福特(Ford) 通用汽車(GM)]發起並創立於1994年
AEC-Q001	零件平均測試指導原則		
AEC-Q002	統計式良品率分析的指導原則		
AEC-Q003	晶片產品的電性表現特性化的指導原則		
AEC-Q100	基於積體電路應力測試認證的失效機理		規範了零件供應商所必須達成的產品品質與可靠度，試驗條件多仍以JEDEC或MIL-STD為主，外加上其他獨立建置的測試手法。
AEC-Q100-001	邦線切應力測試		
AEC-Q100-002	人體模式靜電放電測試		
AEC-Q100-003	機械模式靜電放電測試		
AEC-Q100-004	積體電路閂鎖效應測試		
AEC-Q100-005	可寫可擦除的永久性記憶的耐久性、資料保持及工作壽命的測試		
AEC-Q100-006	熱電效應引起的寄生閘極漏電流測試		
AEC-Q100-007	故障仿真和測試等級		
AEC-Q100-008	早期壽命失效率（ELFR）		
AEC-Q100-009	電分配評估		
AEC-Q100-010	錫球剪切測試		
AEC-Q100-011	帶電器件模式的靜電放電測試		
AEC-Q100-012	12V系統靈敏功率設備的短路可靠性描述		

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簡稱	中文	英文	說明
AEC-Q101	汽車級半導體分立器件應力測試認證		
AEC-Q200	無源器件應力測試標準		
AEC-Q200-001	阻燃測試		
AEC-Q200-002	人體模式靜電放電測試		
AEC-Q200-003	橫樑負載、斷裂強度		
AEC-Q200-004	自恢復保險絲測量程式		
AEC-Q200-005	板彎曲度測試		
AEC-Q200-006	表面貼裝後的剪切強度測試		
AEC-Q200-007	電湧測試		
DPM	百萬缺陷數	defect per million	半導體元件的缺陷率
HRCF	高可靠性認證流程	High Reliability Certified Flow	
ISO-26262	車輛機能安全		
PPAP	生產零件批准程序	Production Parts Approval Process	
SAE J1752	積成電路輻射測量程序		
MIL-STD-883	微電子測試方式和程序		
JEDEC JESD-22	裝氣件可靠性測試方法		
EIA/JESD78	積成電路閉鎖效應測試		
ST	應力測試	stress testing	
UL 94	器件和器具塑料材質零件的易燃性測試		
Zero Defect	零缺陷		

AEC-Q101 元器件规范

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- **AEC - Q101**: Failure Mechanism Based Stress Test Qualification For Discrete Semiconductors
- AEC - Q101 Rev - D1: Failure Mechanism Based Stress Test Qualification For Discrete Semiconductors (base document)
- AEC - Q101-001 - Rev-A: Human Body Model (HBM) Electrostatic Discharge Test
- AEC - Q101-003 - Rev-A: Wire Bond Shear Test
- AEC - Q101-004 - Rev-: Miscellaneous Test Methods
- AEC - Q101-005 - Rev-: Charged Device Model (CDM) Electrostatic Discharge Test
- AEC - Q101-006 - Rev-: Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems

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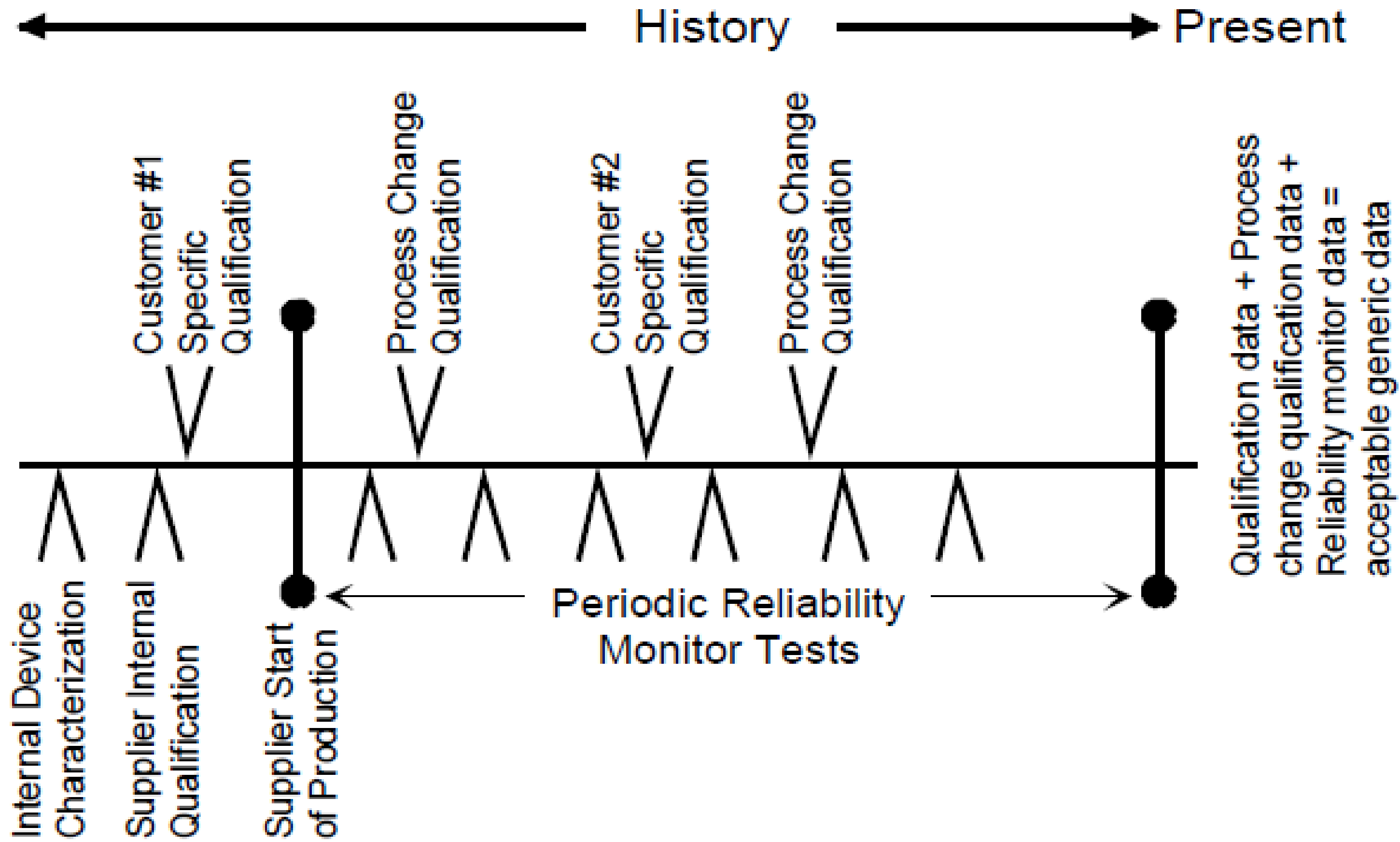

Figure 1: Generic Data Time Line

AEC-Q101 元器件认证列表

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TABLE 2 - QUALIFICATION TEST DEFINITIONS									
#	Stress	Abrv	Data Type	Note	Sample Size per Lot	# of Lots	Accept on # Failed	Reference (current revision)	Additional Requirements
1	Pre- and Post-Stress Electrical Test	TEST	1	NG	All qualification parts tested per the requirements of the appropriate part specification.		0	User specification or supplier's standard specification	Test is performed as specified in the applicable stress reference at room temperature.
2	Pre-conditioning	PC	1	GS	SMD qualification parts before Test # 7, 8, 9, & 10.		0	JESD22 A-113	Performed on surface mount parts (SMDs) prior to Test # 7, 8, 9, & 10 only. TEST before and after PC. Any replacement of parts must be reported.
3	External Visual	EV	1	NG	All qualification parts submitted for testing		0	JESD22 B-101	Inspect part construction, marking and workmanship.
4	Parametric Verification	PV	1	N	25	3 Note A	0	Individual AEC user specification	Test all parameters according to user specification over the part temperature range to insure specification compliance.
5	High Temperature Reverse Bias	HTRB	1	CDGK UVPX	77	3 Note B	0	MIL-STD-750-1 M1038 Method A	1000 hours at the maximum DC Reverse Voltage rated junction temperature specified in the user/supplier specification. The ambient temperature T_A is to be adjusted to compensate for current leakage. TEST before and after HTRB as a minimum. (See note X HTRB.) To be implemented on, or before, April 1, 2014.
5a	AC blocking voltage	ACBV	1	CDGU PY	77	3 Note B	0	MIL-STD-750-1 M1040 Test condition A	1000 hours at the maximum AC blocking voltage and junction temperature specified in the user/supplier specification. The ambient temperature T_A is to be adjusted to compensate for current leakage. TEST before and after ACBV as a minimum.
5b	High Temperature Forward Bias	HTFB	1	DGUZ	77	3 Note B	0	JESD22 A-108	1000 hours at the maximum forward bias. TEST before and after HTFB as a minimum.
5c	Steady State Operational	SSOP	1	CDGU O	77	3 Note B	0	MIL-STD-750-1 M1038 Condition B (Zeners)	1000 hours at rated IZ max, T_A to rated T_J. TEST before and after SSOP as a minimum.

AEC-Q101 元器件认证列表

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TABLE 2 - QUALIFICATION TEST DEFINITIONS (Continued)										
#	Stress	Abrv	Data Type	Note	Sample Size per Lot	# of Lots	Accept on # Failed	Reference (current revision)	Additional Requirements
6	High Temperature Gate Bias	HTGB	1	CDG MUP	77	3 Note B	0	JESD22 A-108	1000 hours at the specified T_J(max) rating, with gate biased at 100% of maximum gate voltage rating indicated in the detail specification with part biased OFF. Can reduce duration to 500 hours through increasing T_J by 25°C. TEST before and after HTGB as a minimum.
7	Temperature Cycling	TC	1	DGU	77	3 Note B	0	JESD22 A-104 Appendix 6	1000 cycles (T_A = minimum range of -55°C to maximum rated junction temperature, not to exceed 150°C). Can reduce duration to 400 cycles using T_A (max) = 25°C over part maximum rated junction temperature or using T_A(max) = 175°C if the maximum rated junction temperature is above 150°C. TEST before and after TC.
7a	Temperature Cycling Hot Test	TCHT	1	DGU1	77	3 Note B	0	JESD22 A-104 Appendix 6	125°C TEST after TC, followed by decap and wire pull on all wires from 5 devices per appendix 6 for parts with internal bond wire sizes 5 mil diameter and less. (Samples may be a sub set of test 7). **To be implemented on, or before, April 1, 2014.**
7a alt	TC Delamination Test	TCDT	1	DGU1	77	3 Note B	0	JESD22 A-104 Appendix 6 J-STD-035	100% C-SAM inspection after TC, followed by decap, inspection or wire pull on all wires from 5 parts per appendix 6 for 5 highest delaminated parts. If C-SAM shows no delaminating, no decap, inspection and wire pull is required. **To be implemented on, or before, April 1, 2014.**
7b	Wire Bond Integrity	WBI	3	DGUF	5	3 Note B	0	MIL-STD-750 Method 2037	500 hours, T_A = maximum rated Tj for bonding of dissimilar metals (e.g., Au/Al), decap and wire pull/bond inspection after WBI on all wires from a maximum of 5 parts. **To be implemented on, or before, April 1, 2014.**
8	Unbiased Highly Accelerated Stress Test	UHAST	1	CDG U	77	3 Note B	0	JESD22 A-118	96 hours at TA=130°C/85%RH. TEST before and after 96 hours UHAST.
8 alt	Autoclave	AC	1	CDG U	77	3 Note B	0	JESD22 A-102	96 hours, TA = 121°C, RH = 100%, 15psig. TEST before and after AC.

AEC-Q101 元器件认证列表

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TABLE 2 - QUALIFICATION TEST DEFINITIONS (Continued)									
#	Stress	Abrv	Data Type	Note	Sample Size per Lot	# of Lots	Accept on # Failed	Reference (current revision)	Additional Requirements
9	Highly Accelerated Stress Test	HAST	1	CDG UV	77	3 Note B	0	JESD22 A-110	96 hours at T_A=130°C/85%RH, or 264hrs TA=110°C /85%RH with part reverse bias at 80% of rated voltage up to a voltage above which arcing in the chamber will likely occur (typically 42V). TEST before and after HAST.
9 alt	High Humidity High Temp. Reverse Bias	H^3TRB	1	DGU V	77	3 Note B	0	JESD22 A-101	1000 hours at T_A = 85°C/85% RH with part reverse biased at 80% of rated breakdown voltage up to a maximum of 100V or limit of chamber. TEST before and after H3TRB as a minimum.
9a	High Temperature High Humidity Bias	HTHHB	1	DGUZ	77	3 Note B	0	JESD22 A-101	1000 hours at T_A = 85°C/85% RH with part Forward biased. TEST before and after H3TRB as a minimum.
10	Intermittent Operational Life	IOL	1	DGTU WP	77	3 Note B	0	MIL-STD-750 Method 1037	Tested per duration indicated in Table 2A. T_A=25°C. Parts powered to insure $\Delta T_J \geq$ 100°C (not to exceed absolute maximum ratings). TEST before and after IOL as a minimum.
10 alt	Power and Temperature Cycle	PTC	1	DGTU W	77	3 Note B	0	JESD22 A-105	Perform PTC if $\Delta T_J \geq$ 100°C cannot be achieved with IOL. Tested per duration indicated for Timing Requirements in Table 2A. Parts powered and chamber cycled to insure $\Delta T_J \geq$ 100°C (not to exceed absolute maximum ratings). TEST before and after PTC as a minimum.
11	ESD Characterization	ESD	1 (HBM) 2 (CDM)	DW	30 each HBM / CDM	1	0	AEC Q101-001, and Q101-005	The supplier must document that the package could not hold sufficient charge to perform the test. TEST before and after ESD.
12	Destructive Physical Analysis	DPA	1	DG	2	1 Note B	0	AEC-Q101-004 Section 4	Random sample of parts that have successfully completed H3TRB or HAST, and TC.
13	Physical Dimension	PD	2	NG	30	1	0	JESD22 B-100	Verify physical dimensions to the applicable user part packaging specification for dimensions and tolerances.
14	Terminal Strength	TS	2	DGL	30	1	0	MIL-STD-750 Method 2036	Evaluate lead integrity of leaded parts only.
15	Resistance to Solvents	RTS	2	DG	30	1	0	JESD22 B-107	Verify marking permanency. (Not required for laser etched parts or parts with no marking.)

AEC-Q101 元器件认证列表

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TABLE 2 - QUALIFICATION TEST DEFINITIONS (Continued)									
#	Stress	Abrv	Data Type	Note	Sample Size per Lot	# of Lots	Accept on # Failed	Reference (current revision)	Additional Requirements
16	Constant Acceleration	CA	2	DGH (1)	30	1 Note B	0	MIL-STD-750 Method 2006	Y1 plane only, 15K g-force. TEST before and after CA.
17	Vibration Variable Frequency	VVF	2	DGH (2)	Items 16 through 19 are sequential tests for hermetic packages. (See note H on Legend page.)			JESD22 B-103	Use a constant displacement of 0.06 inches (double amplitude) over the range of 20Hz to 100 Hz and a 50g constant peak acceleration over the range of 100 Hz to 2 KHz. TEST before and after VVF.
18	Mechanical Shock	MS	2	DGH (3)			0	JESD22 B-104	1500 g's for 0.5mS, 5 blows, 3 orientations. TEST before and after MS.
19	Hermeticity	HER	2	DGH (4)			0	JESD22 A-109	Fine and Gross leak test per individual user specification.
20	Resistance to Solder Heat	RSH	2	DG	30	1	0	JESD22 A-111 (SMD) B-106 (PTH)	TEST before and after RSH. SMD parts shall be fully submerged during test and preconditioned per MSL rating.
21	Solderability	SD	2	DG	10	1 Note B	0	J-STD-002 JESD22B102	Magnification 50x. Reference solder conditions in Table 2B. Apply test method A for through-hole, or both test methods B and D for SMD.
22	Thermal Resistance	TR	3	DG	10 each, pre- & post-change	1	0	JESD24-3, 24-4, 24-6 as appropriate	Measure TR to assure specification compliance and provide process change comparison data.
23	Wire Bond Strength	WBS	3	DGE	10 bonds from min of 5 parts	1	0	MIL-STD-750 Method 2037	Pre- & Post-process change comparison to evaluate process change robustness.
24	Bond Shear	BS	3	DGE	10 bonds from min of 5 parts	1	0	AEC-Q101-003	See attached procedure for details on acceptance criteria and how to perform the test.
25	Die Shear	DS	3	DG	5	1	0	MIL-STD-750 Method 2017	Pre- & Post-process change comparison to evaluate process change robustness.

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TABLE 2 - QUALIFICATION TEST DEFINITIONS (Continued)									
#	Stress	Abrv	Data Type	Note	Sample Size per Lot	# of Lots	Accept on # Failed	Reference (current revision)	Additional Requirements
26	Unclamped Inductive Switching	UIS	3	D	5	1	0	AEC-Q101-004 Section 2	Pre- & Post-process change comparison to evaluate process change robustness (Power MOS and internally clamped IGBTs only).
27	Dielectric Integrity	DI	3	DM	5	1	0	AEC-Q101-004 Section 3	Pre- & Post-process change comparison to evaluate process change robustness. All parts must exceed gate breakdown voltage minimum (Power MOS & IGBT only).
28	Short Circuit Reliability Characterization	SCR	3	DP	10	3 Note B	0	AEC-Q101-006	For smart power parts only.
29	Lead Free	LF	3		-	-	-	AEC-Q005	For all related solderability, solder heat resistance and whisker requirements. **To be implemented on, or before, April 1, 2014.**

* Note: All electrical testing before and after the qualification stresses (including pre-conditioning) are performed to the limits detailed in the individual user specification at room temperature only. For generic qualifications, the supplier's standard specification limits at room temperature may be used.

AEC-Q006 元器件Cu-Wire

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Table 3b: Discrete Qualification Test Requirements based on AEC-Q101

Sequence #	Stress Test / Qualification Step	TC	HAST/H3TRB	IOL	HTRB/HTGB (8)
1	Initial sampling	Sample sizes as required			
2	CSAM @ T0 (1)	Sample sizes as required			
3	Preconditioning to MSLx	3x77	3x77	3x77	---
4	CSAM after PC (1)	3x22	3x22	3x22	---
5	ATE Test	3x77	3x77	3x77	3x77
6	Stress 1X	3x77	3x77	3x77	3x77
7	ATE Test	3x77	3x77	3x77	3x77
8	CSAM post-1X stress (1,5)	3x22	3x22 (6)		
9a	Ball + Stitch/Wedge pull	3x3 (4,7)	3x3 (4,7)	---	---
9b	Ball shear	3x3 (4,7)	3x3 (4,7)	---	---
10	Cross-section	3x1 (7)	3x1 (7)	---	3x1
11	Stress 2X	3x70 (2)	3x70	3x77	3x76
12	ATE Test	3x70 (2,3)	3x70 (3)	3x77 (3)	3x76 (3)
13	CSAM post-2X stress (1)	3x22 (2)	3x22		
14a	Ball + Stitch/Wedge pull	3x2 (2,4)	3x2 (4)	---	---
14b	Ball shear	3x2 (2,4)	3x2 (4)	---	---
15	Cross-section	3x1 (2)	3x1	---	3x1

AEC-Q101 元器件认证计划

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Page 1 of 1	Discrete Semiconductor Component Qualification Plan							Rev: A 4/24/04
User P/N:	N611045BFDAARA		User Component Engineer:	John Doe				
User Spec. #:	ES-N611045BFDAARA		General Specification:	AEC-Q101				
Supplier:	Sam's Discount Semiconductors (SDS)		Supplier Manufacturing Site:	Shanghai, China				
Supplier Generic P/N:	PZT3904		Required PPAP Submission Date:	7/1/2004				
Supplier Internal P/N:	SDF-3417-AR		Family Type:	Bipolar SOT-223, 20 mil square die				
Reason for Qual:	New device qualification							

Item	Test	Test Conditions	Exceptions	Est. Start	Est. Comp.	# Lots	S. S.	Remarks
1	TEST	Electrical Characterization @ 25C		4/1/2004	4/5/2004	all	all	
2	Preconditioning	per AEC-Q101		4/8/2004	4/10/2004	all	all	
3	External Visual	per AEC-Q101		4/11/2004	4/12/2004	all	all	
4	Parametric Verification	Characterization @ -55, 25, & 150C		4/15/2004	4/19/2004	3	30	
5	HTRB	Reverse biased @ 64V		4/22/2004	6/24/2004	3	77	
6	HTGB		N/A Bipolar device					
7	Temperature Cycling		Use attached generic data for this package related test.					generic data uses -65/150C (rather than -55C)
8	Autoclave	Ta = 121C, P = 15PSIG, RH = 100%	Use attached generic data for this package related test.					
9	H3TRB	Reverse biased @ 64V		4/22/2004	6/24/2004	3	77	
10	IOL		T on/off = 2 minutes, 15,000 cycles	4/22/2004	6/24/2004	3	77	SDS internal standard
11	ESD	per AEC-Q101		4/22/2004	6/24/2004	1	30	
12	DPA	per AEC-Q101		6/24/2004	6/24/2004	3	2	2 ea from H3TRB and TC only.

Comments:

1. Supplier requests 1 lot qualification of this device type in addition to attached rel reports fo similar parts to total 3 lots.
   Rel Report #23-602 (PZT3906, the PNP compliment of this part) and #23-665 (PZTA62 NPN Darlington with larger 35 MIL die)
2. In addition, the die is qualified in SOT-23 version of this device, the SOT-223 package is qualified with larger (35 MIL) bipolar die (N611002BFDAARA & N611007BFDBARA).
3. Attached quarterly reliability results for 2002 & 2003 on generic PZT3904.
4. These devices all share the same wafer and assembly processes.
5. Tests 14-23 covered by annual SOT-223 packaging qual last approved 11/03.

Prepared by (supplier):		Approved by (User):	
Typed/Printed		Typed/Printed	
Signature		Signature	
Title		Title	

* Note: This plan is only an example and does not represent all the required tests in this document.

Figure A3.1: Example of Discrete Semiconductor Qualification Test Plan

AEC-Q101 元器件测试结果表格

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Supplier Sam's Discount Semiconductors		User Part Number N611045BFDAARA			
Name of Laboratory SDS Qual Lab		**Part Description** Bipolar SOT-223 Transistor			
Test #	**Test Description**	**Test Conditions**	**# Lots**	**# Tested**	**# Failed**
2	Preconditioning	Per Spec	3	77	0
3	External Visual	Per Spec	3	381	0
5	HTRB	Reverse Biased @ 64V; Tj = 150C	3	77	0
9	H3TRB	Reverse Biased @ 64V; 85C/85%RH	3	77	0
10	IOL	T on/off = 2 min, 15K Cycles	1	77	0
11	ESD	Per Spec	1	30	N/A
12	DPA	Per Spec	3	2	0

Note: This listing of test results is only an example and does not represent all the tests in this document.

Figure A4.1: Environmental Test Summary Example

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AEC-Q101 工艺变更对应测试

Table 2 Test #	3	4	5/abc	6	7	7ab	8/alt	9/alt/a	10/alt	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
Test Name / Change	External Visual	Parametric Verification	HTRB / ACBV / HTFB / SSOP	High Temp. Gate Bias	Temperature Cycle	TC Hot / TC Delam / WBI	UHAST / Autoclave	HAST / H^3TRB / HTHHB	IOL / PTC	ESD Characterization	Destruct. Phy. Analysis	Physical Dimensions	Terminal Strength	Resistance to Solvents	Constant Acceleration	Vibration	Mechanical Shock	Hermeticity	Resist. to Solder Heat	Solderability / AEC-Q005	Thermal Resistance	Wire Bond Strength	Wire Bond Shear	Die Shear	Unclamp. Induct. Switch	Dielectric Integrity	Short Circuit Reliability Characterization	NOTES
DESIGN																												
Wafer Thickness		•	•		•	•			•		•								x		•	•	•					F
Wafer Diameter		•	•	•																								
Die Size		•	•		•				•	E	•								•		•			•	M		•	F
Layout		•	•	•	3				•	E	3														M		•	
Field Termination		•	•		•		•	•		E	•														M			
WAFER FAB																												
Wafer Source		•	•					•	•												•				9,M			R
Lithography		•	4	4				6,7														1						P
Diffusion		•	5,6	5			6	6		•	6														M			PR
Doping Profile/Schottky Barrier		•	5,0							•															M			R
Ion Implantation		•	5,6	•			6	6		•	6														M			PR
Polysilicon		•	•	•	•					E	•														M	•	•	P
Metallization (Top side)		•	8		•	•	•	•	•	E	•								•			•	•				•	
Metallization (Back side)		•			•			•	•										•		•			•				
Passivation/Glassivation		•	•	•	•		•	•	•	•	•											•						
Oxide		•		•	7		6	6	•	E	6,7															•		
Epitaxic Growth		•	•																						M			R
Etch		•	6	4			6,7	6,7			6,7											1,7			8,M	4		
Backside Operation		•			•		•	•	•										•		•			•				A
Fab Site Transfer		•	•	•	•	•	•	•	•	E	•										•	•	•	•	M	•		AIPRS
ASSEMBLY																												
Die Overcoat			•	•	•		•	•	•		•							H				•						
Leadframe Plating/Lead Finish	D				C		C	C				D		D				H		D	C	2C		C				
Leadframe Mat'l/Source	•				•	•	•	•	•			•	•					H	•	•	•	2		•			•	AFX
Package/LF Dimension					•			•	•			•						H			•			•			•	
Wire Bonding		•			•	•		•	•		•								•			•	•				•	
Die Scribe/Separation/Saw		•			•				•																			
Die Preparation/Clean		•			•		•	•														•		•				X
Die Attach		•			•		•	•	•									H	•		•			•			•	AX
Encapsulation Material	•	•	•	•	•	•	•	•	•		•	•		B				H	•	•	•					•		AFG
Encapsulation Process	•		•	•	•	•	•	•	•		•	•		B				H	•	•								AG
Hermetic Sealing	H				H		H	H			H		H		H	H	H	H	H									
New Package	•	•	•	•	•	•	•	•	•	•	•	•	•	B	H	H	H	H	•	•	•			•		•	•	
Test Process/Sequence		•																										
Package Marking														B														
Assembly Site Transfer	•	•	•	•	•	•	•	•	•		•	•	•	•			H	H	•	•		•	•	•				AGISX

A Acoustic Microscopy H Hermetic part only 1 If bond pads are affected
6 For field termination changes
B If not laser etched I Infant Mortality Rate 2 Verify #2 (package) post 7 For passivation changes
C Only for Leadframe Plating change M Power MOS/IGBT parts only 3 Only for changes at the periphery 8 For contact changes
D Only for Lead Finish change P CV Plot (MOS only) 4 Only for oxide etches or
etches prior to oxidation
9 For epitaxial changes
E If Applicable R Spreading Resistance Profile 0 Required for Schotthy
F Finite Element Analysis S Steady State Mortality Rate 5 For source or channel region Barrier changes changes
G Glass Transition Temperature X X-Ray

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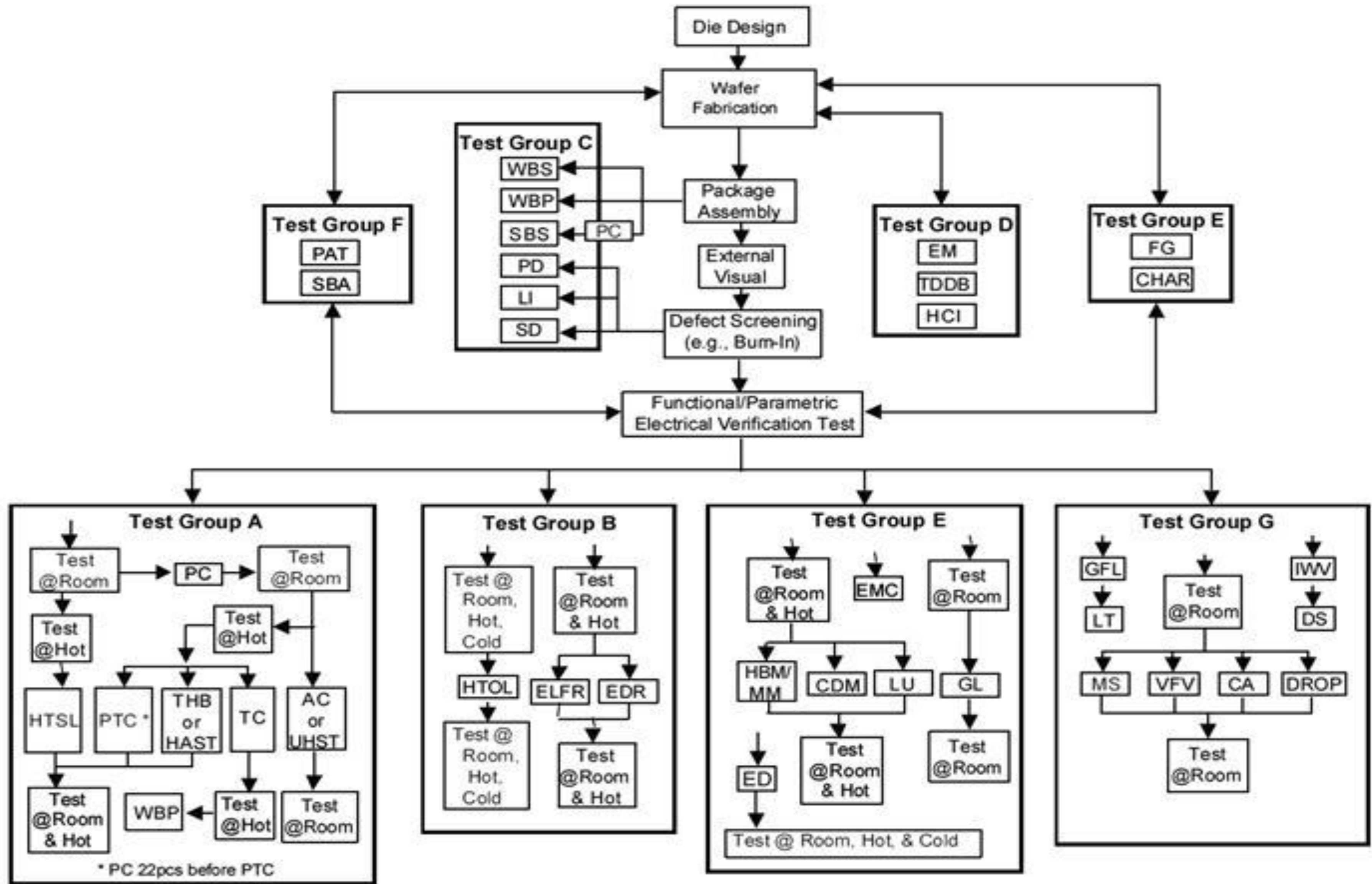
要求通過AECQ-100的車用電子零配件哉要列表：

車用一次性記憶體、電源降壓穩壓器、車用光電耦合器、三軸加速規感測器、視訊解碼器、整流器、環境光感測器、非易失性鐵電存儲器、電源管理IC、嵌入式快閃記憶體、DC/DC穩壓器、車規網路通訊設備、液晶驅動IC、單電源差動放大器、電容接近式開關、高亮度LED驅動器、非同步切換器、600V IC、GPS IC、ADAS高級駕駛員輔助系統晶片 、GNSS接收器、GNSS前端放大器..等

AEC-Q100車用IC產品驗證流程圖：



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AEC-Q100類別與測試：

說明：AEC-Q100規範7大類別共41項的測試

群組A-加速環境應力測試(ACCELERATED ENVIRONMENT STRESS TESTS)共6項測試，包含：PC、THB、HAST、AC、UHST、TH、TC、PTC、HTSL

群組B-加速生命週期模擬測試(ACCELERATED LIFETIME SIMULATION TESTS)共3項測試，包含：HTOL、ELFR、EDR

群組C-封裝組裝完整性測試(PACKAGE ASSEMBLY INTEGRITY TESTS)共6項測試，包含：WBS、WBP、SD、PD、SBS、LI

群組D-晶片製造可靠性測試(DIE FABRICATION RELIABILITY TESTS)共5項測試，包含：EM、TDDB、HCI、NBTI、SM

群組E-電性驗證測試(ELECTRICAL VERIFICATION TESTS)共11項測試，包含：TEST、FG、HBM/MM、CDM、LU、ED、CHAR、GL、EMC、SC、SER

群組F-缺陷篩選測試(DEFECT SCREENING TESTS)共11項測試，包含：PAT、SBA

群組G-腔封裝完整性測試(CAVITY PACKAGE INTEGRITY TESTS)共8項測試，包含：MS、VFV、CA、GFL、DROP、LT、DS、IWV

測試項目簡稱說明:

AC：壓力鍋
CA：恆加速
CDM：靜電放電帶電器件模式
CHAR：特性描述
DROP：包裝跌落
DS：晶片剪切試驗
ED：電分配
EDR：非易失效儲存耐久性、數據保持性、工作壽命
ELFR：早期壽命失效率
EM：電遷移
EMC：電磁兼容
FG：故障等級
GFL：粗/細氣漏測試
GL：熱電效應引起閘極漏電
HBM：靜電放電人體模式
HTSL：高溫儲存壽命
HTOL：高溫工作壽命
HCL：熱載流子注入效應
IWV：內部吸濕測試
LI：引腳完整性
LT：蓋板扭力測試
LU：閂鎖效應
MM：靜電放電機械模式
MS：機械衝擊
NBTI：富偏壓溫度不穩定性
PAT：過程平均測試
PC：預處理
PD：物理尺寸
PTC：功率溫度循環
SBA：統計式良率分析
SBS：錫球剪切
SC：短路特性描述
SD：可焊性
SER：軟誤差率
SM：應力遷移
TC：溫度循環
TDDB：時經介質擊穿
TEST：應力測試前後功能參數
TH：無偏壓濕熱
THB、HAST：有施加偏壓的溫濕度或高加速應力試驗
UHST：無偏壓的高加速應力試驗
VFV：隨機振動
WBS：焊線剪切
WBP：焊線拉力

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AEC-Q100 溫濕度試驗條件整理：

THB(有施加偏壓的溫濕度，依據JESD22 A101)：85°C/85%R.H./1000h/bias
HAST(高加速應力試驗，依據JESD22 A110)：
130°C/85%R.H./96h/bias、110°C/85%R.H./264h/bias
AC(壓力鍋，依據JEDS22-A102)：121°C/100%R.H./96h
UHST(無偏壓的高加速應力試驗，依據JEDS22-A118)：110°C/85%R.H./264h
TH(無偏壓濕熱，依據JEDS22-A101)：85°C/85%R.H./1000h

TC(溫度循環，依據JEDS22-A104)：
等級0：-50°C←→150°C/2000cycles
等級1：-50°C←→150°C/1000cycles
等級2：-50°C←→150°C/500cycles
等級3：-50°C←→125°C/500cycles
等級4：-10°C←→105°C/500cycles

PTC(功率溫度循環，依據JEDS22-A105)：
等級0：-40°C←→150°C/1000cycles
等級1：-65°C←→125°C/1000cycles
等級2～4：-65°C←→105°C/500cycles

AEC-Q100 溫濕度試驗條件整理：

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HTSL(高溫儲存壽命，JEDS22-A103)：

塑料封裝零件：

等級0：150℃/2000h

等級1：150℃/1000h

等級2～4：125℃/1000h or 150℃/5000h

陶瓷封裝零件：200℃/72h

HTOL(高溫工作壽命，JEDS22-A108)：

等級0：150℃/1000h

等級1：150℃/408h or 125℃/1000h

等級2：125℃/408h or 105℃/1000h

等級3：105℃/408h or 85℃/1000h

等級4：90℃/408h or 70℃/1000h

ELFR(早期壽命失效率，AEC-Q100-008)：

Grade 0: 48 hours at 150° C or 24 hours at 175° C

Grade 1: 48 hours at 125° C or 24 hours at 150° C

Grade 2: 48 hours at 105° C or 24 hours at 125° C

Grade 3: 48 hours at 85° C or 24 hours at 105° C

Grade 4: 48 hours at 70° C or 24 hours at 90° C

1.2.1 Military

MIL-STD-750 Test Methods for Semiconductor Devices

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1.2.2 Industrial

UL-STD-94 Test for Flammability of Plastic Materials of Parts in Devices and Appliances.
JEDEC JESD-22 Reliability Test Methods for Packaged Devices
J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.
J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
JESD22-A113 Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
J-STD-035 Acoustic Microscopy for Nonhermetic Encapsulated Electronic Components

1.2.3 Automotive

AEC-Q001 Guidelines for Part Average Testing
AEC-Q005 Pb-Free Test Requirements
AEC-Q101-001 ESD (Human Body Model)
AEC-Q101-003 Discrete Component Wirebond Shear Test
AEC-Q101-004 Miscellaneous Test Methods
• Unclamped Inductive Switching; • Dielectric Integrity; • Destructive Physical Analysis
AEC-Q101-005 ESD (Charged Device Model)
AEC-Q101-006 Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems

1.2.4 Other

QS-9000; ISO-TS-16949

AEC - Q003 IC Characterization

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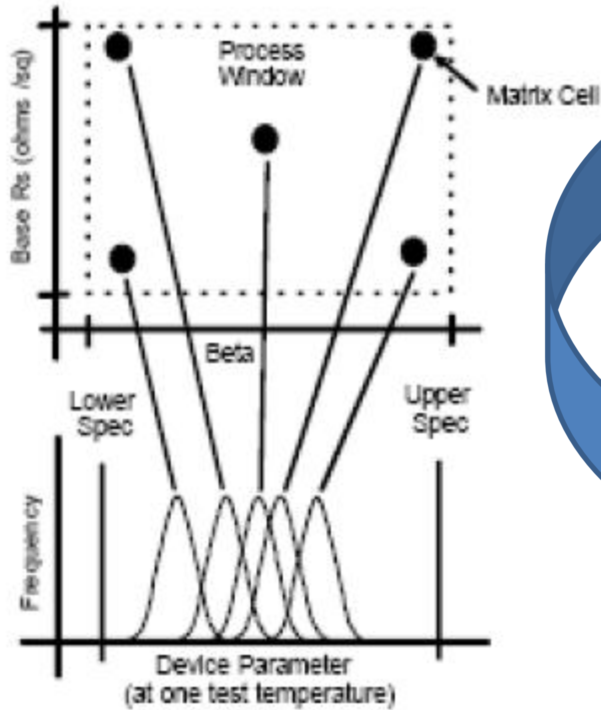

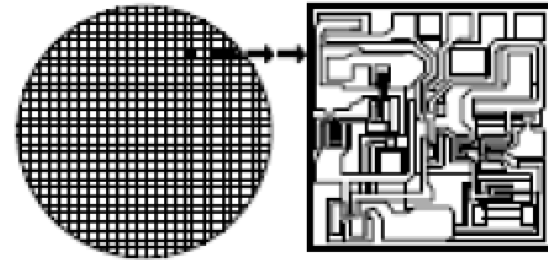

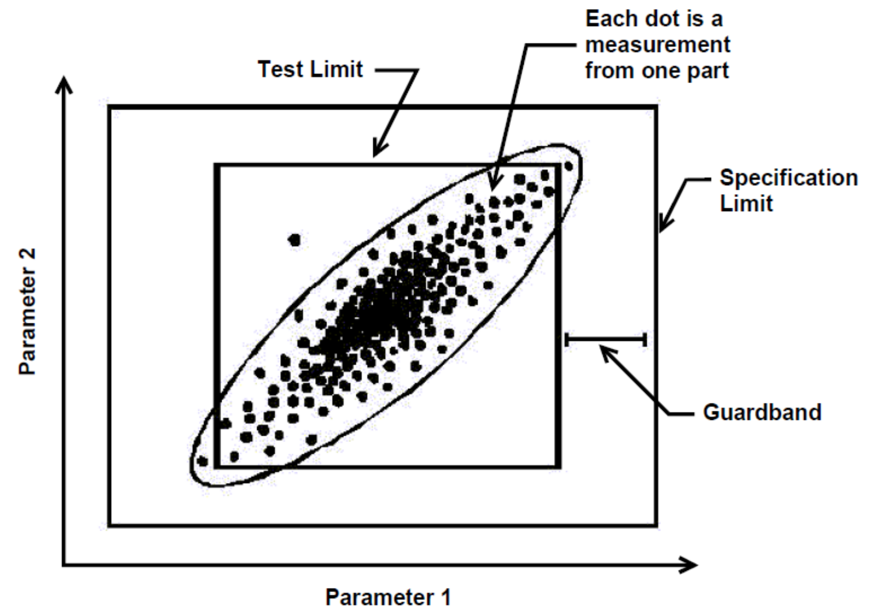

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Table 1: Short Term CPK and PPM Estimation

Cpk	Sigma	PPM
0.67	2.00	45500
1.00	3.00	2700
1.33	4.00	63
1.67	5.00	0.57
2.00	6.00	0.002

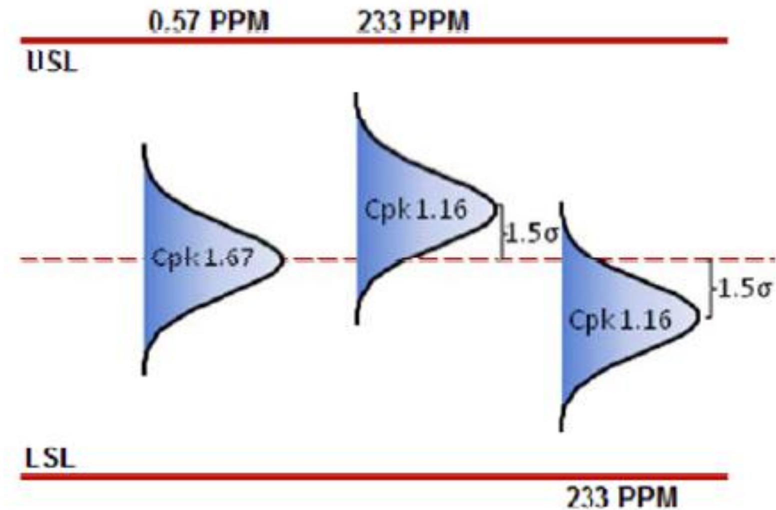

Table 2: CPK and PPM Estimation (with a 1.5 Sigma process drift)

Short term		Assuming a long term 1.5 sigma shift		
Cpk	Sigma	Sigma with shift	Cpk with shift	PPM
0.67	2.00	0.50	0.17	308,538
1.00	3.00	1.50	0.50	66,807
1.33	4.00	2.50	0.83	6,210
1.67	5.00	3.50	1.17	233
2.00	6.00	4.50	1.50	3

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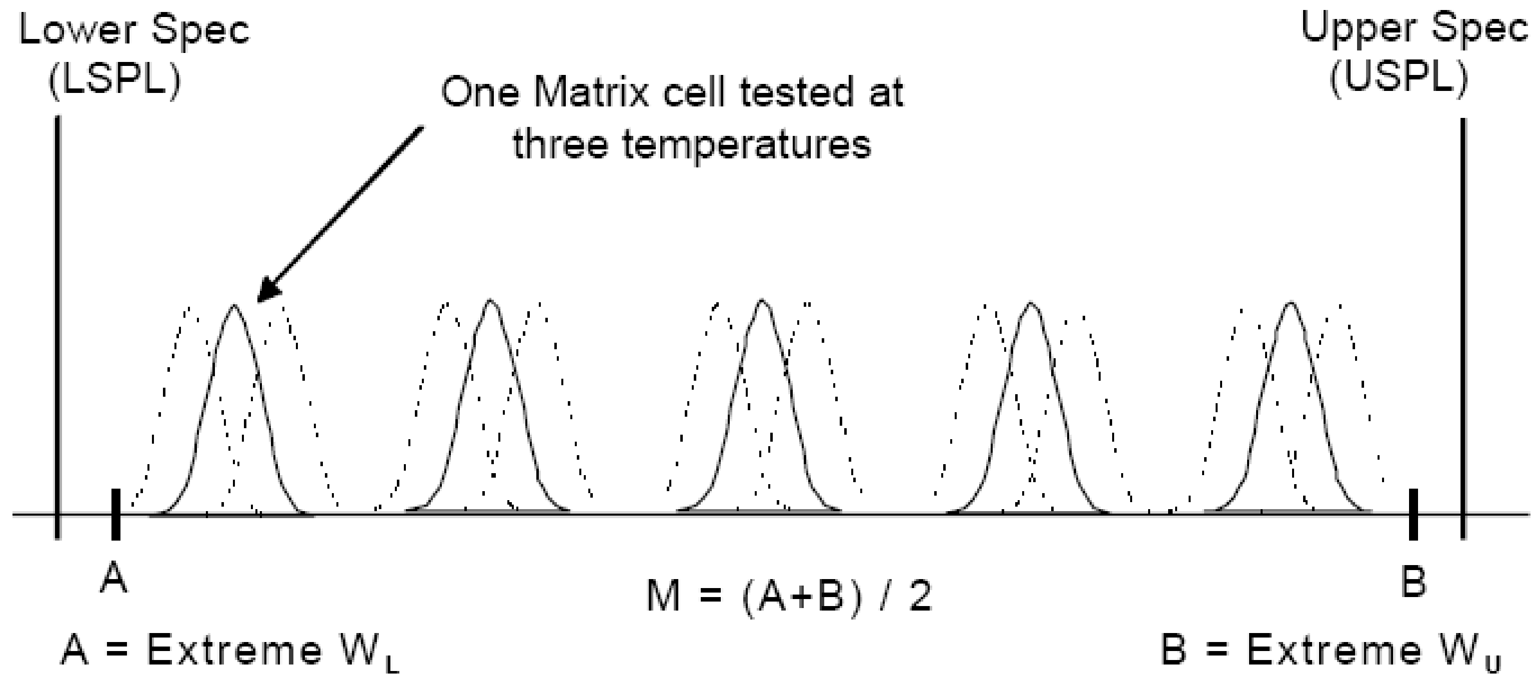
Corners Across 3 Temperatures



AEC - Q002 Statistical Yield Analysis

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SYL_1 = Mean - 3 Sigma

SBL_1 = Mean + 3 Sigma

Hold for Eng-Review

SYL_2 = Mean - 4 Sigma

SBL_2 = Mean + 4 Sigma

Hold for Risk Assessment

AEC - Q004 DRAFT Zero Defect

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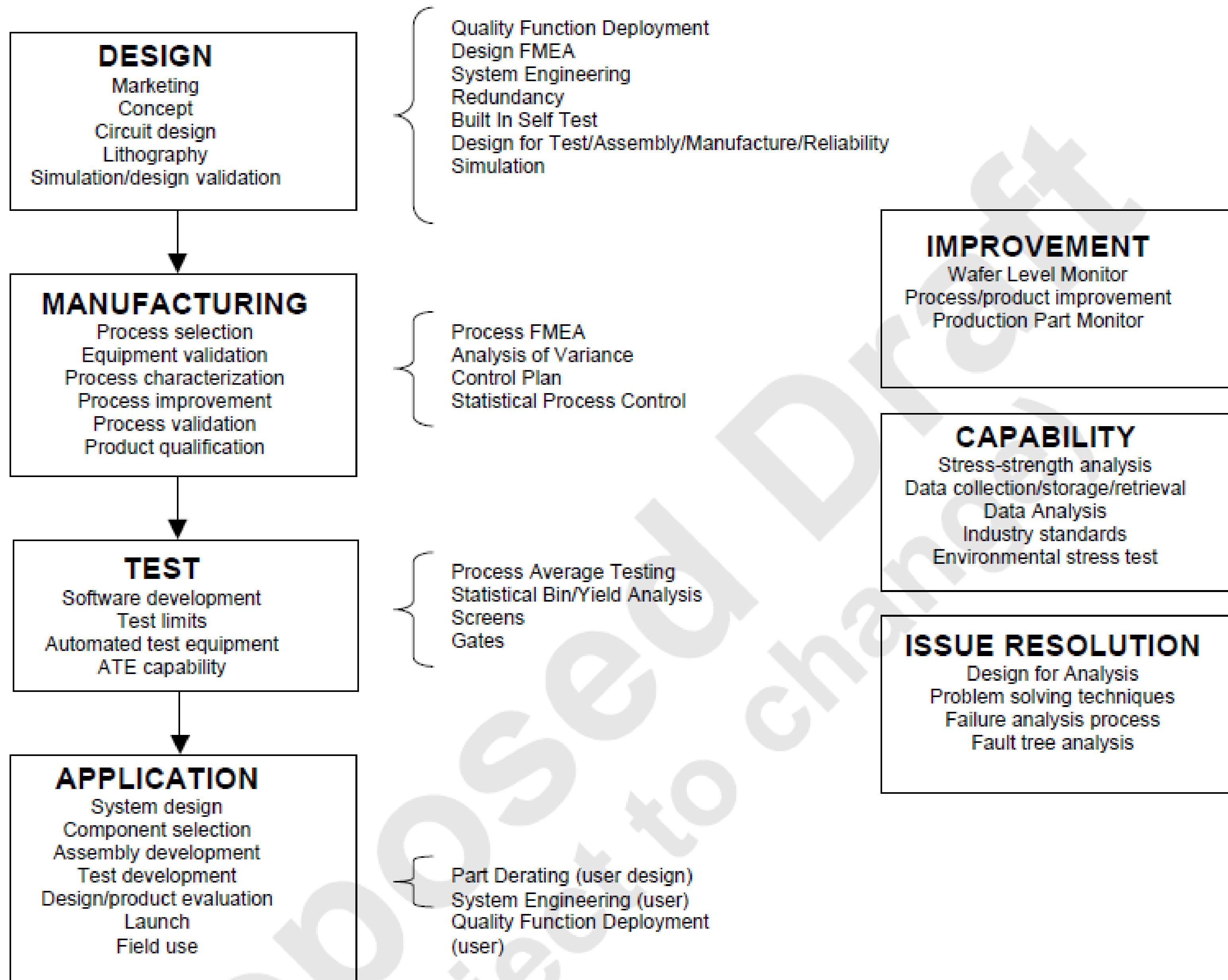

Proposed Draft subject to change

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THANKS