APPLICATION NOTE

A 45 Watt Adapter Power Supply

AN01033

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Abstract

The present application note describes a typical notebook adapter power supply, based on a GreenchipII™ controller, the TEA1533. The features of this controller are elaborated in full detail and a possible design strategy is given to obtain the basic component values. The performance of the final application-board is tested in order to check if the specification is met. The results are presented in tabular or graphical form.

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1. INTRODUCTION

1.1 A TYPICAL ADAPTER POWER SUPPLY

The present application note will focus on a Switched Mode Power Supply (SMPS) intended for a general 45W notebook adapter. The most important features of such a SMPS are listed below

- Flat and compact design.
- Universal mains input, i.e.V_{ac} = 90V…265V.
- Low voltage high current output, i.e. 12V/4A.
- High efficiency(η>0.83) in order to limit the ambient temperature to acceptable values.
- Low cost.

A more detailed specification is given in APPENDIX 1. As will be clear, this specification can be used for different type of AC adapters as well (e.g. inkjet printer adapters, game console adpaters etc.). Those power supplies have the same output characteristics, i.e. a relatively low voltage at a high current.

Different topologies (resonant LLC, hard-switching flyback, Quasi Resonant flyback etc.) can be used to realize a SMPS as described above, however the combination of universal mains, low cost and high efficiency more or less implies for a Quasi Resonant flyback converter

- A wide input voltage span can be covered since both the duty-cycle and switching frequency are used to control the output power.
- Low cost due to the low component count (only one secondary diode and one primary MOSFet).
- High efficiency because of the resonant behavior (soft/semi-soft switching of the primary MOSFet).

The GreenChipII flyback controller can perfectly be used to address those specification items and cover all the necessary protections as well without the use of additional external components.

1.2 THE GREENCHIP^{TM}II FAMILY

The GreenChip^{TM}II (TEA1507, TEA1533) is a variable frequency SMPS controller designed for a Quasi-Resonant Flyback converter operating directly from the rectified universal mains (see APPENDIX 2 for the complete electrical schematic). The topology is in particular suitable for TV and Monitor Supplies, but can be used for high efficient Consumer Electronics SMPS as well. The power supply operates in a critical conduction mode (border continuous/discontinuous mode of operation) at nominal output loads including zero/low voltage switching (ZVS/LVS). The ZVS/LVS is achieved by the resonant behavior of the voltage across the power switch and is therefore often referred to as Quasi-Resonant mode of operation. A novel valley detection circuitry implemented in the controller results in exact valley switching under all conditions.

The control method used in the GreenChip^{TM}II is of the Current Mode Control type, which has the benefit of inherent line frequency ripple rejection. Control takes place by comparing the sensed primary current with the error voltage that is present on the Ctrl pin (V_{CTRL}) to generate the primary “on” time. At higher and nominal output powers the switching frequency is depended on the input voltage and the output load. Since the MOSFet

is switched on only if the transformer core is completely demagnetized and the drain voltage is at it's minimum (valley detection). The GreenChip^{TM}II is intended to be used in combination with secondary control (opto-coupler feedback) resulting in a very accurate control of the output voltage at all load conditions and load transients.

Standard two different types of stand-by modes are provided. The first is Reduced Frequency Mode of Operation, which is detected by means of the control voltage and minimizes the switching losses at low output loads. This feature enables the possibility for no load power consumption levels below 1W for this type of power supplies and no additional circuitry is needed. A second standby mode for extreme no load power consumptions is called Burst Mode of Operation, which needs only little additional circuitry. The latter one is explained in detail in Application Note AN00047. If no microprocessor signal is present to initiate Burst Mode of Operation, one can use the Automatic Controlled Burst Mode which is only present in the TEA1533.

The key features of the GreenChip^{TM}II are summarized below in no special order

Distinctive features

- Operates from universal mains input $85V_{AC} - 276V_{AC}$
- High level of integration leads to a very low external component count
- Soft (re)Start to prevent audible noise (externally adjustable)
- Leading Edge Blanking (LEB) for current sense noise immunity
- Mains dependent operation enabling level (Mlevel) (externally adjustable)

Green features

- On-chip start-up current source, which is switched "off" after start-up to reduce the power consumption
- Valley (zero/low voltage) switching for minimal switching losses
- Frequency Reduction at low output powers for improved system efficiency (power consumption < 1W)
- Burst mode operation (Automatic Controlled Burst Mode) for extreme low, no load power levels

Protection features

- Safe-Restart mode for system fault conditions
- Under Voltage Protection (UVLO) for foldback during overload
- Continuous mode protection by means of demagnetization detection
- Accurate Over Voltage Protection (OVP) (external adjustable)
- Cycle-by cycle Over Current Protection (OCP)
- Input voltage independent Over Power Protection (OPP)
- Short Winding Protection (SWP)
- Maximum T_{on} Protection
- Over Temperature Protection (OTP)

These features enable the power supply engineer to design a reliable and cost effective SMPS with a minimum number of external components and the possibility to deal with the high efficiency requirements.
Since the microprocessor signal which normally initiates Burst Mode is not present in adapter power supplies the Automatic Burst Mode Control of the TEA1533 is used. Therefore the remainder of this application note will focus on the TEA1533.

2. FUNCTIONAL DESCRIPTION OF THE TEA1533

2.1 START-UP SEQUENCE

As soon as the rectified line voltage V_{DC} has increased up to the Mains Dependent Operation Level (Mlevel), the internal Mlevel switch will be opened and the high voltage start-up current source will be enabled. This current source will charge the V_{CC} capacitor as depicted in Fig. (2.1). The soft start switch is closed at the moment the V_{CC} capacitor voltage level reaches 7V (typ.). This level initiates the charging of the soft start capacitor, V_{SS}, up to a voltage level of 500mV with a typical current of $60mA$. In the mean time the V_{CC} capacitor is continued to be charged by the internal high voltage current source in order to reach the V_{CC} start-up level. Once the V_{CC} capacitor is charged to the start-up voltage level (11V typ.) the TEA1533 controller starts driving the external MOSFet and both the high voltage and the soft start current sources are switched off. Resistor R_{SS} will discharge the soft start capacitor, C_{SS}, resulting in an increasing amplitude of the primary peak current to its steady state value in normal mode of operation. This smooth transition in current level will limit audible noise caused by magnetostriction of the transformer core material. The time constant of the decreasing voltage across C_{SS}, which is representing the increasing primary peak current, can be controlled with the RC combination R_{SS}/C_{SS}. To use the total soft start window, R_{SS} should be chosen

$$R_{SS} > \frac{V_{OCP}}{I_{SS}} = \frac{500\text{mVtyp}}{60\mu\text{Atyp}} = 8.7\text{k}\Omega,$$

(2.1)

and from

$$i_s = C_{V_{CC}} \frac{dV_{CC}}{dt_s} \rightarrow dt_s = \frac{C_{V_{CC}} \left(V_{CC\_start} - V_{CC\_softstart}\right)}{i_s},$$

$$i_{ss} = C_{SS} \frac{dV_{C_{SS}}}{dt_{ss}} \rightarrow dt_{ss} = \frac{C_{V_{C_{SS}}} V_{C_{ss}}^{\max}}{i_{ss}},$$

$$dt_{ss} < dt_s \rightarrow C_{SS} < 0.4C_S.$$

(2.2)

a appropriate soft start capacitor can be chosen, in order to be sure that C_{SS} is pre-charged to it's maximum level of 500mV. During start-up phase the V_{CC} capacitor will be used to deliver the necessary energy to power the TEA1533 up till the moment the auxiliary winding overtakes.

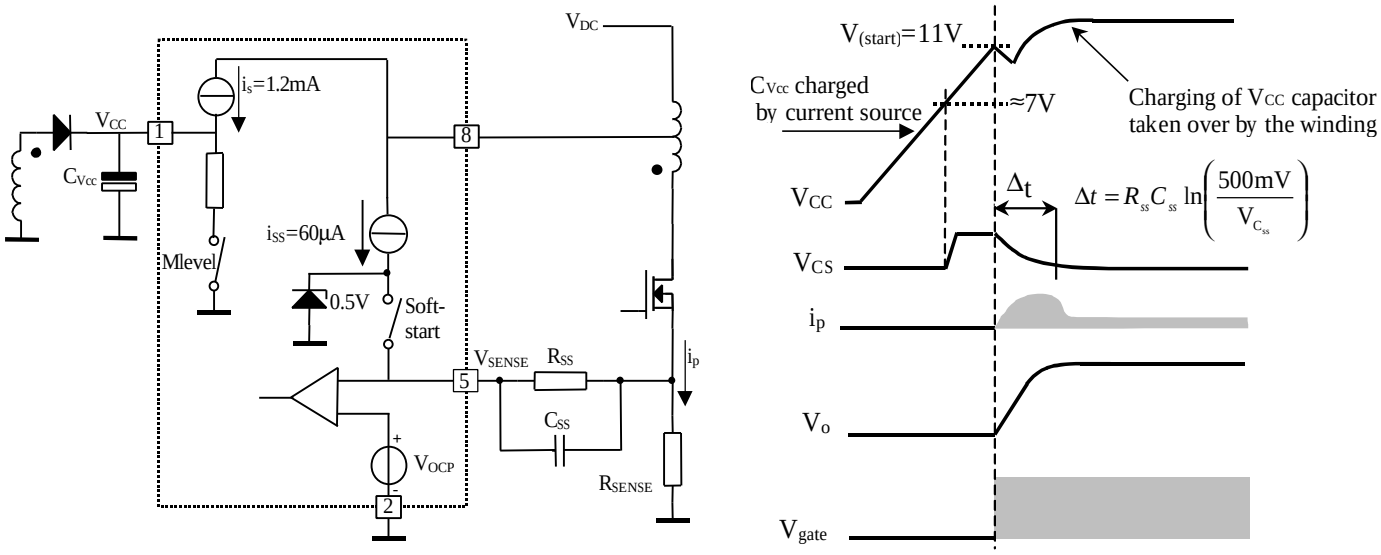


Fig. (2.1) Start-up charging of C_{Vcc} and soft start control.

2.2 MULTI MODE OPERATION

In order to achieve the highest efficiency possible at various output loads, the TEA1533 is able to operate in six different modes, which are listed below in order from maximum output power to no load.

1. Quasi-Resonant (QR-mode) mode of operation
2. Fixed Frequency (FF-mode) mode of operation
3. Frequency Reduction (VCO-mode) mode of operation
4. Minimum Frequency (MF-mode) mode of operation
5. Automatic Burst (AB-mode) mode of operation
6. Forced Burst (FB-mode) mode of operation

The latter one is not automatically invoked but must be initiated by means of little additional circuitry.

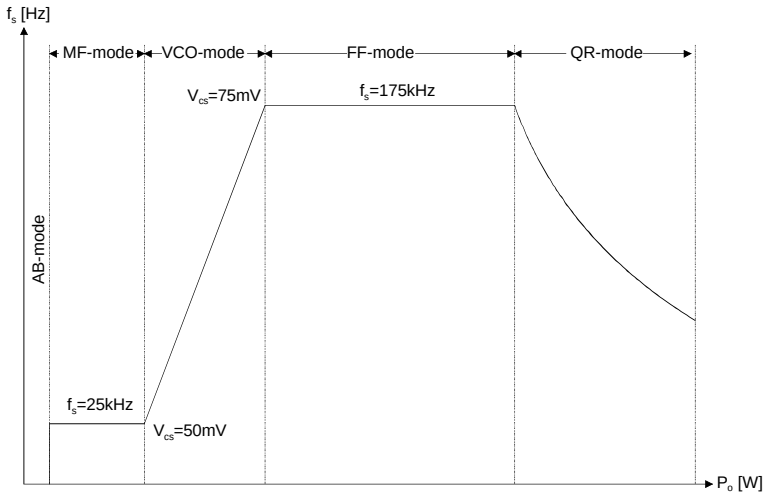


Fig. (2.2) The switching frequency versus output power. Each power level corresponds with a different mode of operation.

QR-mode is the most appropriate mode of operation at high output loads. Switching on of the MOSFet is only allowed at the minimum of the drain-source voltage (LVS/ZVS) which reduces the switching losses ($P_{sw} = \frac{1}{2} C_{ds} V_{ds}^{\ 2} f_s$) resulting in an improved efficiency performance. EMI will be improved for two reasons when operating in QR-mode. First the current spike due to discharging of the resonant capacitor, C_{ds}, is lower, since the voltage at switching on is lower due to LVS/ZVS. Secondly the switching frequency is modulated with the double mains frequency and can be approximated by

$$f_s = \frac{h}{2 P_0 L_p} \left(\frac{N V_{DC} \left(V_0 + V_F \right)}{N V_{DC} + V_0 + V_F} \right).$$

(2.3)

This effect causes the EMI spectrum to be spread over the frequency band, rather than being concentrated on a single frequency value.

FF-mode is an improvement on the normal behavior of a QR-mode power supply that tends to increase the switching frequency to very high levels at the moment the output power is reduced. In FF-mode the switching frequency is fixed to a predefined level avoiding this unwanted frequency increase. Valley switching is still active in this mode of operation, increasing the overall efficiency of the power supply.

FR-mode is implemented to decrease the switching losses at low output loads. In this way the efficiency at low output powers is increased, which enables lower power consumption The voltage at the Ctrl pin determines where the frequency reduction starts. An external Ctrl voltage of 1.425 V corresponds with an current sense level of 75mV. The frequency will be reduced linear with the current sense level (At current sense levels higher than 75mV, Ctrl voltage < 1.425V, the oscillator will run on maximum frequency f_{oscH} = 175kHz typically). At a current sense level of 50mV, V_{CTRL} = 1.450V, the frequency is reduced to the minimum level of 25kHz. Valley switching is still active in this mode.

MF-mode
At current sense levels below 50mV (V_{CTRL}>1.450V), the minimum frequency will remain at 25 kHz.

AB-mode
At current sense levels below 41mV (V_{CTR}>1.459V), switch on of the external MOSFet is inhibited and as a result switching cycles are left out. As soon as the control voltage has dropped below 1.459V, the power supply starts switching again. The time constant of the feedback loop will determine the number of switching cycles.

FB-mode
As soon as the V_{CTRL} voltage level is pulled up to a level higher then 3.8V (typ.) and a minimum current of 16mA for 30µs (typ.) is injected the controller stops switching as well. The difference to AB-mode of operation is that the controller resumes switching after a complete restart cycle, i.e. the V_{cc} capacitor has to be discharged to UVLO and recharged to V_{cc_start}.

2.3 SAFE-RESTART MODE

This mode is introduced to prevent destruction of components due to excessive heat generation during system faults (fault condition tests) and is used for Burst mode of operation as well. The Safe-Restart mode will be invoked after being triggered by the activation of one of the next functions

1. Over Voltage Protection (Not TEA1533P type, because of latched protection)
2. Short Winding Protection
3. Maximum “on time” Protection
4. V_{CC} reaching UVLO level
5. Detecting a pulse for Burst mode
6. Over Temperature Protection (Not TEA1533P type, because of latched protection)

When entering the Safe-Restart mode the output driver is immediately disabled and latched, that means the SMPS stops switching and is locked in this state. The auxiliary winding will not charge the V_{CC} capacitor anymore and the V_{CC} voltage will drop until UVLO is reached. To recharge the V_{CC} capacitor the internal current source (i_s) will be switched on to initiate a new start-up sequence as described in paragraph 2.1. The TEA1533 will remain in its operation in Safe Restart mode until the fault condition or the Burst mode triggers pulses are removed.

2.4 PROTECTIONS

2.4.1 Demagnetization sense

This feature guarantees discontinuous conduction mode operation at any time in any mode of operation. This function prevents the transformer core to saturate and continuous mode of operation during initial start-up and when overloading the output. The demag(netization) sense is realized by an internal circuit that guards the

voltage (V_{demag}) at pin 4 that is connected to auxiliary winding by resistor R_1. Fig. (2.3)shows the circuit and the idealized waveforms across this winding.

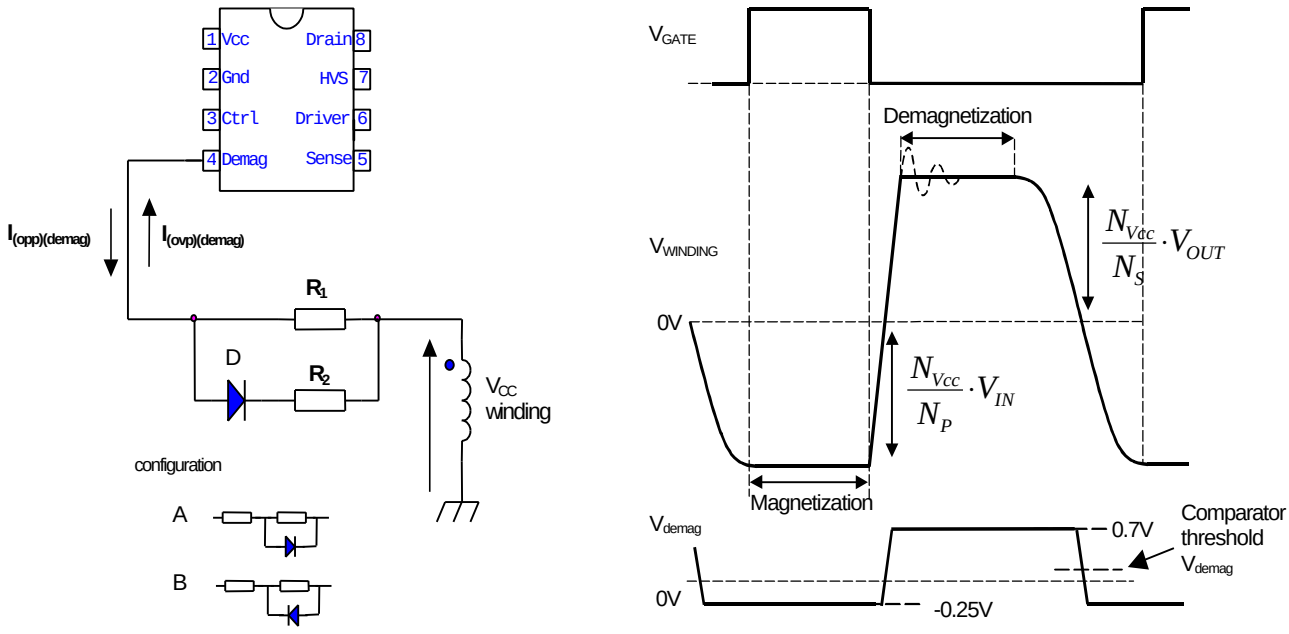


Fig. (2.3) Demagnetisation sensing and relevant waveforms.

As long as the secondary diode is conducting (demagnetization of transformer), the auxiliary winding voltage is positive (flyback stroke). In this case V_{demag} is also positive and clamped at a level of 700mV. The controller will force the driver output to remain in “off” mode as long as the voltage at pin 4 is positive and above 100mV. This means that the switching frequency has the possibility to decrease in case of start-up or overload condition. After demagnetization the reflected output voltage at the auxiliary winding starts oscillating since it is well coupled with the primary winding and therefore reflecting the $L_p C_{ds}$ -oscillation, which occurs after the flyback stroke. When the voltage condition $V_{demag} < 100mV$ is met the controller will wait for valley detection to allow the start of a new switching cycle.

In order to limit the total number of pins, novel OVP and OPP functions are implemented using the same IC pin. These two protections determine the resistor values of R_1 and R_2.

NOTE: There are two configurations to be considered. Dependent on the highest resistor value (R_1 or R_2) one should choose the direction if the diode. See configuration A and B in Fig. (2.3).

2.4.2 Over Voltage Protection

The Over Voltage Protection ensures that the output voltage will remain below an external adjustable level. This is realized by sensing the reflected output voltage across the auxiliary winding by means of the current flowing into the demagnetization pin. This reflected voltage is related to the output voltage via to the turns ratio of the auxiliary winding (n_a) and the secondary winding (n_s). The maximum output voltage is set by the resistor value R_1 that determines the positive current flowing into the demagnetization pin of the TEA1533. This current is compared with an internal threshold level of $60mA$ (typ.) and exceeding this level will trigger the OVP function. R_1 can be calculated with

$$R_1 = \frac{\frac{n_a}{n_s}\left(V_{o\_OVP} + V_F\right) - V_{dem\_clamp\_pos}}{i_{dem\_OVP}},$$

(2.4)

in which n_a is the number of auxiliary turns, n_s is the number of secondary, V_{o_OVP} is the OVP output voltage level, $V_{dem\_clamp\_pos}$ is the positive clamp voltage of demagnetization input (700mV typ.), V_F is the forward voltage drop of the auxiliary diode and i_{dem_OVP} is the current threshold of the OVP protection (60µA typ.)

After triggering the OVP function, the driver is disabled and the controller enters, depending on the type, or Safe-Restart mode (TEA1533AP) or is latched (TEA1533P). The controller will remain in this state as long as an over-voltage condition is present at the output. In case of a latched OVP, operation only recommences when the V_{CC} voltage level drops below a level of about 4.5V. The dashed line in Fig. (2.3)shows a more practical waveform of the auxiliary winding. The ringing is caused by the $L_s C_{ds}$ oscillation. To compensate this ringing (load dependent) the current into the demagnetization pin is integrated over the flyback time interval. This method increases the accuracy of the OVP detection level and prevents false triggering.

2.4.3 Over Current and Over Power Protection

The maximum output power limitation needs some special attention when using a Quasi-Resonant converter. The maximum output power is not only function of the primary peak current $\hat{i}_p$, but of the input voltage, V_{DC} as well. Eq.(2.5) shows the relation between input voltage and output power (the resonance time is neglected).

$$P_{O\_MAX} = \eta \cdot \frac{\hat{i}_p}{2} \cdot \left(\frac{N\left(V_o + V_F\right)V_{DC}}{N\left(V_o + V_F\right) + V_{DC}} \right),$$

(2.5)

The maximum output power will increase with the input voltage when the OCP level would be a fixed level. To prevent over dimensioning of all the secondary power components an internal OCP compensation is used to get an independent OPP level. This compensation is realized by sensing the input voltage level via the auxiliary winding, since $V_a = \left(n_a / n_p\right)V_{DC}$ during the primary “on” time. A resistor is connected between this winding and

the demagnetization pin. During magnetization of the transformer the reflected input voltage is present at this winding (see Fig. (2.3)). A negative current into this pin is used to compensate the OCP level. Fig. (2.4)shows the relation between the negative current and OCP level.

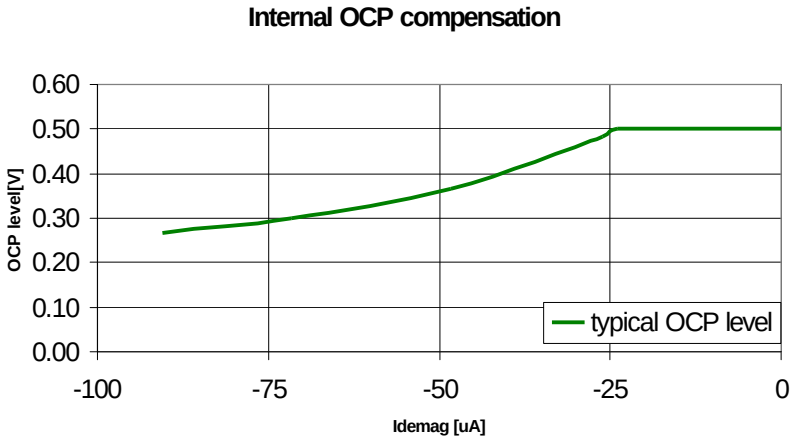


Fig. (2.4) Internal OCP compensation

The current threshold level where the controller starts to compensate the OCP level is fixed at - 24µA. This threshold level is used to set the external resistor value at the minimum input voltage, leading to

$$R_2 = \frac{V_{DC\_\min}\frac{n_a}{n_p} - V_{dem\_clamp\_neg}}{i_{dem\_OPP}},$$

(2.6)

in which n_a is the number of auxiliary turns, n_p is the number of primary turns, $V_{DC\_\min}$ is the minimum DC input voltage, $V_{dem\_clamp\_neg}$ is the negative clamp voltage of demagnetization pin (-250mV typ.) and i_{dem_OPP} is the internal current threshold of OPP correction (-24µA typ.)

2.4.4 Short Winding Protection

The short winding protection is implemented as a protection for shorted transformer windings, for example in case of a secondary diode short. In this case the primary inductance is shorted out and the primary current starts to rise at very high rate (only limited by the leakage inductance) after switch-on of the MOSFET. An additional comparator (fixed threshold of $V_{swp} = 880\text{mV}$) implemented in the IC will detect this fault condition by sensing the voltage level (via pin 5) across the sense resistor. Immediately the driver is disabled and the controller enters the Safe-Restart mode. This protection circuit is activated after the leading edge blanking time (LEB).

2.4.5 LEB and maximum "on-time"

The LEB (Leading Edge Blanking) time is an internally fixed delay preventing false triggering of the comparator due to current spikes that are present at the current sense voltage. This delay determines the minimum "on time" of the controller. This minimum on time together with the minimum switching frequency and the primary inductance defines the minimum input power at which the output voltage is still in regulation. Because this minimum frequency is low it is possible to run at extremely low loads (without any pre-load).
The IC will protect the system against an "on-time" longer then 50µs (internally fixed maximum "on-time"). When the system requires on times longer than 50µs, a fault condition is assumed, and the controller enters the Save-Restart mode.

2.4.6 Over Temperature protection

When the junction temperature exceeds the thermal shutdown temperature (typ 140°C), the IC will disable the driver and will or enter Safe Restart mode or is latched. When the V_{CC} voltage drops to UVLO, the V_{CC} capacitor will be recharged to the V_{start} level. If the temperature is still too high, the V_{CC} voltage will drop again to the UVLO level (Safe-Restart mode). This mode will persist until the junction temperature drops 8 degrees typically below the shutdown temperature.

2.4.7 Mains dependent operation enabling level

To prevent the supply from starting at a low input voltage, which could cause audible noise, a mains detection is implemented (Mlevel). This detection is provided via pin 8 (no additional pin needed), that detects the minimum start-up voltage between 60V and 100V. As previous mentioned the controller is enabled between 60V and 100V. This level can be adjusted by connecting a resistance in series with the drain pin, which increases the level by Ri_{drain} volts, which is roughly equal to $1\text{V}/\text{k}\Omega$
An additional advantage of this function is the protection against a disconnected buffer capacitor (C_{IN}). In this case the supply will not be able to start-up because the V_{CC} capacitor will not be charged to the start-up voltage.

2.5 PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
Vcc	1	This pin is connected to the supply voltage. An internal current source charges the V_{CC} capacitor and a start-up sequence is initiated when the voltage reaches a level of 11V. The output driver is disabled when the voltage gets below 9V(UVLO). Operating range is between 9V and 20V.
Gnd	2	This pin is ground of the IC.
Ctrl	3	This pin is connected to the feedback loop. The pin contains two functions, i.e. primary current control and standby mode selection. Between 1V and 1.425V it controls the on time. The frequency is reduced starting from a level of 1.425V up till 1.450V, where the frequency is equal to the minimum frequency of the oscillator (25kHz). From a level of 1.459V and up switching cycles are left out and Automatic

		Burst mode of operation starts. Above a threshold of 3.5V it is possible to initiate Forced Burst mode standby via a current pulse (16mA@30µs).
Demag	4	This pin is connected to the V_{CC} winding. The pin contains three functions. During magnetization the input voltage is sensed to compensate the OCP level for OPP (independent of input voltage). During demagnetization the output voltage is sensed for OVP and a comparator is used to prevent continuos conduction mode when the output is overloaded.
Sense	5	This pin contains three different functions. Soft start, protection levels OCP (OPP) and SWP. By connecting an R_{SS} and C_{SS} between the sense resistor and this pin it is possible create a Soft start. Two different protection levels of 0.5V(this OCP level depends on the Demag current) and 0.88V(fixed SWP level) are implemented.
Driver	6	This pin will drive the switch (MOSFET). The driver is capable of sourcing and sinking a current of respectively 125mA and 540mA.
HVS	7	This is a High Voltage Spacer (keep this pin floating)
Drain	8	This pin is connected to the drain of the switch or center-tap of the transformer depending on the voltage (BV_{DSS} = 650V). The pin contains three functions. The Mlevel that enables the controller between 60V and 100V input voltage, supply the start-up current and valley detection for zero/low voltage switching.

Table 2.1 Pin description

3. DESIGN OF A 45 WATT ADAPTER POWER SUPPLY

3.1 DESIGN PARAMETERS

In order to dimension all the components of the power supply, the data, which is given below, is used.

Name	Value	Dimension	Description
V_{AC_min}	90	V	The minimum AC input voltage from the mains
V_{AC_max}	265	V	The maximum AC input voltage from the mains
f_{l_min}	47	Hz	The minimum line frequency
f_{l_max}	63	Hz	The maximum line frequency
V_{DC_min}	100	V	The minimum DC voltage across the input capacitor
V_{DC_max}	375	V	The maximum DC voltage across the input capacitor
V_{AC_nom}	110	V	The nominal AC input voltage for mains interruptions and lifetime calculations
V_{DC_drop}	100	V	The absolute minimum voltage during mains interruptions
V_o	12	V	Output voltage
P_{o_min}	6	W	Minimum output power
P_{o_nom}	24	W	Nominal output power
P_{o_max}	45	W	Maximum output power
η	0.85		Targetted efficiency of the power supply
B_{max}	300	mT	Maximum core excitation
A_e	$106 \cdot 10^{-6}$	m^2	Effective core cross-sectional area
V_f	500	mV	Forward voltage drop of the secondary diode

Table 3.1 Design data

3.2 INPUT CIRCUITRY

3.2.1 Input Capacitor

The capacitance value of the input capacitor is

$$C_i = \frac{P_{o\_max}\left(p - \arccos\left(\frac{V_{DC\_min}}{\sqrt{2}V_{AC\_min}}\right)\right)}{hpf_{l\_min}\left(\left(\sqrt{2}V_{AC\_min}\right)^2 - V_{DC\_min}{}^2\right)}, \quad (3.1)$$

resulting in a input capacitance value of 143µF. The voltage rating of this capacitor is equal to the closest standard series value above V_{DC_max} = 375V resulting in a 385V or a 400V input capacitor.

The mains interruption time can be calculated with

$$t = \frac{C_i}{2P_{o\_nom}}\left(\left(\sqrt{2}V_{AC\_nom}\right)^2 - V_{DC\_drop}^2\right),$$

(3.2)

and after substituting the values $t = 44\text{ms} > 1/f_{l\_\min} = 21\text{ms}$ which is more than enough.

3.3 FLYBACK TRANSFORMER

3.3.1 General design consideration

The flyback transformer is dimensioned in a different way as described in Application Note AN00047. As pointed out, to get the most out of LVS/ZVS, the reflected voltage NV_o should be as high as possible to force the lowest possible drain voltage at the moment of switching on the MOSFet. In case of a low output voltage application as described in this application note, one has to increase the turns ratio $N = n_p/n_s$ a lot in order to accomplish this. This has a consequence for the secondary peak current, which will increase as well, according to

$$\hat{i}_s = \frac{n_p}{n_s}\hat{i}_p,$$

(3.3)

resulting in a higher RMS current in the output capacitor. An optimum should be found between high NV_o values and low secondary RMS currents in order to use the benefits of LVS and cheap capacitors and secondary diode losses.

For this project the low profile EQ30 transformer is chosen, in order to solve the height restriction.

3.3.2 Transformer Design, first Approximation

The transformer calculation starts with defining the boundary conditions. The first boundary conditions are the maximum turns ratio N_{max}

$$N_{\max} = \frac{V_{BR} - V_{DC\_\max} - \Delta V}{V_o + V_F},$$

(3.4)

in which V_{BR} is the MOSFet break voltage and ΔV is the overshoot caused by the leakage inductance of the transformer. The latter one is estimated to 125V. N_{max}'s counterpart is the minimum turns ratio N_{min}

$$N_{\min} = \frac{V_{DC\_\max}}{V_R - V_o - V_F},$$

(3.5)

in which V_R is the maximum reverse voltage of the secondary diode. Substituting the data of Table 3.1 in Eqs.(3.4)-(3.5) results in

$$N_{max} = 8,$$
$$N_{min}(V_R = 45\text{V}) = 11.5,$$
$$N_{min}(V_R = 60\text{V}) = 7.9,$$
$$N_{min}(V_R = 100\text{V}) = 4.3.$$

As a first shot *N* will be fixed to 8. This results in the most benefit of ZVS/LVS.

Given this turns ratio, one is able to calculate the duty cycle of the MOSFet's "on" / "off" sequence using

$$d_p = \frac{N(V_o + V_F)}{N(V_o + V_F) + V_{DC}},$$

(3.6)

which is by approximation valid at the border of continuous/discontinuous mode of operation. Substituting *N* = 8 and the data of Table 3.1 in Eq. (3.6) results in $d_p = 0.5$. In critical conduction mode is by definition is valid

$$n_p = Nn_s,$$

(3.7)

which can be used to calculate the number of primary turns if the number of secondary turns is known.

An approximation for the minimum switching frequency f_s is given by

$$f_{s\_min} = \frac{(V_o + V_F)(1 - d_{p\_max})}{B_{max} A_e n_s}.$$

(3.8)

A table can be made containing different n_s versus f_s combinations using Eq. (3.8). The results are listed in Table 3.2.

n_s [turns]	f_s [kHz]
1	196
2	98
3	65
4	49
5	39

Table 3.2

There are two reasons to use a low number of turns (n_s as well as n_p)

1. The limited winding area due to the height restriction
2. Efficiency reasons. The lower the number of turns, the less RMS losses in the transformer windings.

Three turns is a good compromise, taking the switching frequency into account, resulting in 24 primary turns.

The primary inductance can be calculated with

$$L_p = \frac{V_{DC\_\min}{}^2 d_{p\_\max}{}^2 h}{2P_{o\_\max} f_{s\_\min}},$$

(3.9)

resulting in $L_p = 363mH$.

DESIGN SUMMARY: $L_p = 363mH$, $n_p = 24\,\text{turns}$ and $n_s = 3\,\text{turns}$.

3.3.3 The Resonance Capacitor, C_{DS}

For EMI reasons, one should limit the switch off drain-source voltage rise to $6\text{kV}/m\text{s}$. Using this rule of thumb C_{ds} can be calculated with

$$\hat{i}_p = \frac{V_{DC} d_p T}{L_p},$$

(3.10)

and

$$\frac{dV}{dt} = \frac{\hat{i}_p}{C_{ds}}.$$

(3.11)

Substitution of Eq. (3.10) in Eq (3.11) and solving for C_{ds} leads to

$$C_{ds} = \frac{dt}{dV}\frac{V_{DC} d_p T}{L_p},$$

(3.12)

resulting in $C_{ds} > 350\text{pF} \rightarrow C_{ds} = 470\text{pF}$.

3.3.4 Transformer Design, final Calculation

In Eq. (3.6) and Eq. (3.8) the extra time needed for the L_pC_{ds}-oscillation is neglected, since L_p was unknown. More accurate formulas are

$$t_{osc} = \frac{p}{\sqrt{\frac{1}{L_p C_{ds}} - \left(\frac{R_{L_p}}{2L_p}\right)^2}},$$

$$d_{p\_\max} T = \frac{L_p P_{o\_\max}}{h V_{D\bar{C}\min}^2}\left(1 + \frac{n_s V_{DC\_\min}}{n_p\left(V_o + V_F\right)}\sqrt{h}\right) + \frac{1}{2}\sqrt{\left(\frac{2L_p P_{o\_\max}}{h V_{D\bar{C}\min}^2}\left(1 + \frac{n_s V_{DC\_\min}}{n_p\left(V_o + V_F\right)}\sqrt{h}\right)\right)^2 + \frac{8L_p P_{o\_\max} t_{osc}}{h V_{DC\_\min}^2}},$$

$$d_{s\_\max} T = \frac{n_s V_{DC\_\min}}{n_p\left(V_o + V_F\right)}\sqrt{h}\, d_{p\_\max} T.$$

(3.13)

Substitution of the data from Paragraph 3.3.2 in Eq. (3.13) results in the three time intervals of one switching period, $d_p T = 8.2ms$, $d_s T = 7.3ms$ and $t_{osc} = 1.3ms$. These results can be used for calculating the real switching frequency, primary peak current and core excitation

$$f_{s\_\min} = \frac{1}{d_{p\_\max} T + d_{s\_\max} T + t_{osc}},$$
$$\hat{i}_{p\_\max} = \frac{V_{DC\_\min} d_{p\_\max} T}{L_p},$$
$$B_{\max} = \frac{V_{DC\_\min} d_{p\_\max}}{A_e f_{s\_\min} n_p},$$

(3.14)

resulting in $f_{s\_\min} = 60\text{kHz}$, $\hat{i}_{p\_\max} = 2.23\text{A}$ and $B_{\max} = 310\text{mT}$ .As will be clear the switching frequency is reduced, since the $L_p C_{ds}$ -oscillation time is added. The core excitation is therefore increased to a level above the limiting 300mT. There are two options to solve this problem

1. Increase the number of primary turns. This will influence the turns ratio n_p / n_s and the maximum drain-source voltage will be increased. To overcome that, the secondary number of turns should be increased as well. This solution will end up with to many windings given the limited winding area.
2. Decrease the primary inductance, which automatically increases the switching frequency (Eq. (3.9)) and as a result decrease the core excitation (Eq. (3.14)).

According the equations the effects are more or less linear, so a 10% to 15% lower primary inductance value would result in a 10% to 15% lower core excitation. Using Eqs. (3.13) and (3.14) once more and substitution of $L_p = 300mH$ leads to $f_{s\_\min} = 70\text{kHz}$, $\hat{i}_{p\_\max} = 2.3\text{A}$ and $B_{\max} = 265\text{mT}$. The switching period is in this case split up in $d_p T = 6.9ms$, $d_s T = 6.2ms$ and $t_{osc} = 1.2ms$.

The total number of auxiliary windings can be calculated using

$$n_a = \frac{V_{CC}}{V_o} n_s .$$

(3.15)

Substituting the datasheet values $V_{CC\_\max} = 18\text{V}$ and $V_{CC\_UVLO} = 9.3\text{V}$ results in

$$\left\lceil \frac{V_{CC\_UVLO}}{V_o} n_s \right\rceil = 3 < n_a < \left\lfloor \frac{V_{CC\_\max}}{V_o} n_s \right\rfloor = 4 .$$

(3.16)

Due to peak-rectification $n_a = 3$ will be sufficient.

DESIGN SUMMARY: $L_p = 300mH$, $n_p = 24\,\text{turns}$, $n_a = 3\,\text{turns}$ and $n_s = 3\,\text{turns}$.

3.4 THE CURRENT SENSE RESISTOR

The current sense resistor, R_{CS}, can be calculated with

$$R_{CS} = \frac{V_{CS\_max}}{\hat{i}_{p\_max}},$$

(3.17)

resulting, after substitution of $V_{cs\_max} = 520\text{mV}$ and $\hat{i}_{p\_max} = 2.23\text{A}$, $R_{CS} = 233\text{m}\Omega$. A headroom of 15% will be accomplished by using a parallel combination of 0.33Ω, 1Ω and 1.8Ω.

3.5 THE PRIMARY MOSFET

The "on"-resistance, R_{DS_on}, and the break down voltage, V_{BR}, are in this stage the most important parameters for the design. The gate charge, Q_g, needed to completely switch "on" the MOSFet will be considered later. The value for the break down voltage was already fixed to 600V, since the design implies for a low NV_o-value. The reflected voltage NV_o present on the drain winding has a value of 100V, which results in ZVS at minimum mains. As a consequence one can neglect the switching losses and only the conduction losses remain, according to

$$P_c = i^2_{p\_RMS} R_{DS\_on}.$$

(3.18)

The allowable thermal rise of the MOSFet (casing) is set to practical value of 45^oC ($T_{\max} - T_{amb\_\max} = 100^o - 55^o\text{C} = 45^o\text{C}$) The thermal resistance of the heatsink used is $22\,\text{K/W}$, so the maximum allowable dissipation in the MOSFet is 2W. The primary RMS current can be calculated using the primary peak current since

$$i_{p\_RMS\_\max} = \hat{i}_{p\_\max}\sqrt{\frac{d_{p\_\max}}{3}},$$

(3.19)

and is equal to 0.76A. resulting in a $R_{DS\_on}(100^o\text{C})$ of 3.5Ω. Translating this result back to the standard datasheet value of 25^oC using

$$R_{DS\_on}(T) = R_{DS\_on}(25^o\text{C})1.007^{T-25},$$

(3.20)

results in $R_{DS\_on}(25^o\text{C}) = 2\Omega$ (STP5NB60 or equivalent type)

The switching losses at high mains are equal to

$$P_s = \frac{1}{2} C_{ds} V_{ds}{}^2 f_s,$$

(3.21)

and after substitution of the given data result in a worse case loss of 2.45W.

For a graphical representation of the losses in the MOSFet see Fig. (3.1).

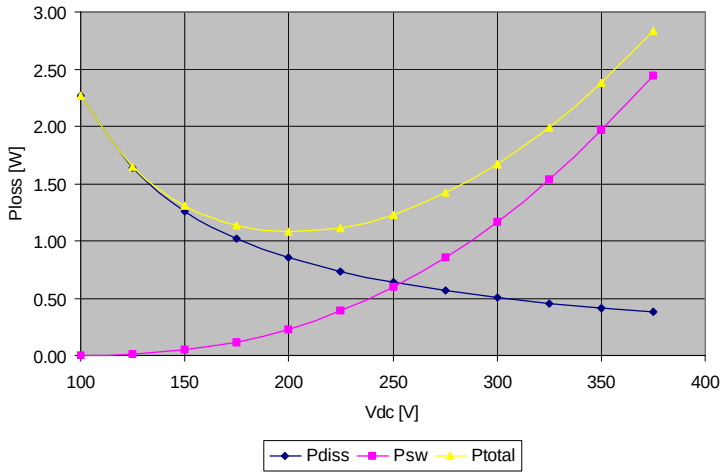


Fig. (3.1) Power losses of the MOSFet as function of the input voltage.

3.6 THE SECONDARY DIODE

The secondary diode is designed with two parameters in mind: the maximum reverse voltage across the diode and the maximum current through the diode. The reverse voltage can be cast with

$$V_{reverse}^{\max} = \frac{V_{DC\_\max}}{N} + V_o ,$$

(3.22)

and is in this case equal to 59V. This means that a 60V diode will do.

For the secondary RMS and average current we can write respectively

$$i_{s\_RMS} = N i_{p\_RMS} = \hat{i}_p N \sqrt{\frac{d_p}{3}},$$
$$i_{s\_AV} = \frac{N \hat{i}_p (1 - d_p)}{2}.$$

(3.23)

A disadvantage of the flyback topology is the fairly high secondary maximum peak current, in this case 18A. The secondary diode has to be chosen with these high currents in mind. For this project a 60V Schottky diode (30CTQ60) is chosen with a series resistance of approximately 5mΩ, an average forward voltage drop of 0.5V and a reverse current of 2mA.

The losses in the secondary diode can be approximated by

$$P_{loss} = V_F i_{s\_AV} + R_s i_{s\_RMS}^2 + \frac{d_p (V_{DC} + V_o) i_{rev}}{N}.$$

(3.24)

The losses in the secondary diode at maximum output power as function of the input voltage are depicted in Fig. (3.2).

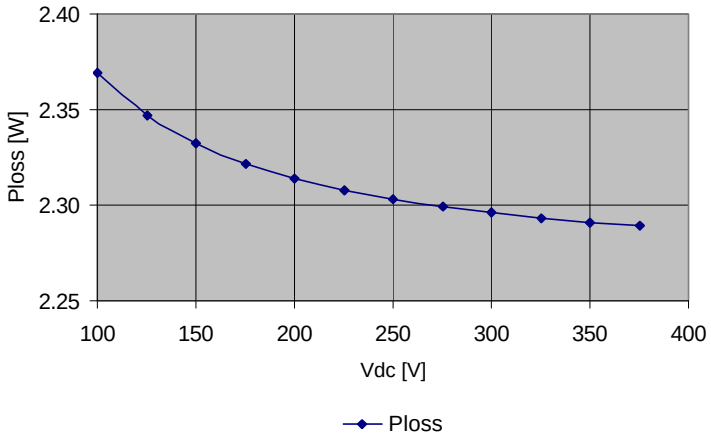


Fig. (3.2) The losses in the secondary diode as function of the input voltage. As will be clear, the series resistance of the Schottky diode is dominant.

3.7 SECONDARY CAPACITOR

The RMS ripple current of the secondary capacitor can be estimated with

$$i_{C\_RMS\_\max} = i_o \sqrt{\frac{4}{3d_{p\_\max}} - 1},$$

(3.25)

resulting in $i_{C\_RMS\_\max} = 4.8\text{A}$. Due to this high RMS ripple current and the low building height of the power supply, miniaturised low ESR type capacitors are used, in this case the parallel combination of two Rubycon ZL-type 25V-1000µF ($12.5 \times 20\text{mm}$) capacitors. The voltage rating of 25V will create enough headroom during over voltage situations.

3.8 PROTECTIONS

The over-voltage (open loop) protection and the maximum current sense level correction are both adjustable with the current flowing in and out the demagnetisation pin as depicted in Fig. (2.3).

The over voltage protection is activated at the moment the current flowing into the demagnetisation pin is greater then $60m\text{A}$. This current level is controlled by R_{dem_OVP}, or in equation form

$$R_{dem\_OVP\_\max} = \frac{\left(V_{o\_OVP} + V_F\right)\frac{n_a}{n_s} - V_{dem\_clamp\_pos}}{60mA} = \frac{(15+0.5)\frac{3}{3} - 0.7}{60mA} = 247k\Omega,$$

$$R_{dem\_OVP\_\min} = \frac{\left(V_o + V_F\right)\frac{n_a}{n_s} - V_{dem\_clamp\_pos}}{60mA} = \frac{(12+0.5)\frac{3}{3} - 0.7}{60mA} = 196k\Omega.$$

(3.26)

The current drawn from the demagnetisation pin controls the maximum current sense level. This circuit should be dimensioned in such a way that no compensation occurs below $V_{DC\_\min}$, or in equation form

$$R_{dem\_OCC} = \frac{V_{DC\_\min}\frac{n_a}{n_p} - V_{dem\_clamp\_neg}}{24mA} = \frac{100\frac{3}{24} - 0.5}{24mA} = 500k\Omega\ .$$

(3.27)

Option A from Fig. (2.3) is used since $R_{dem\_OCC} > R_{dem\_OVP}$. The latter one must me adjusted since an additional forward voltage drop is introduced,

$$R_{dem\_OVP\_\max} = \frac{\left(V_{o\_OVP} + V_F\right)\frac{n_a}{n_s} - V_{dem\_clamp\_pos} - V_F}{60mA} = \frac{(15+0.5)\frac{3}{3} - 0.7 - 0.7}{60mA} = 235k\Omega,$$

$$R_{dem\_OVP\_\min} = \frac{\left(V_o + V_F\right)\frac{n_a}{n_s} - V_{dem\_clamp\_pos} - V_F}{60mA} = \frac{(12+0.5)\frac{3}{3} - 0.7 - 0.7}{60mA} = 185k\Omega.$$

(3.28)

Using a 200kΩ resistor will be a good compromise between safe OVP and false triggering.

Since R_{dem_OCC} is made with two resistors, its value is equal to

$$R_{dem\_OCC} = 500k\Omega - 200k\Omega = 300k\Omega\ .$$

(3.29)

These resistor values are a good starting point, but have to be fine tuned in the application. The parasitic capacitor of the diode can not be neglected anymore due to the high ohmic resistor values. For that reason a voltage division is added in the final circuit diagram resulting in more low ohmic values for the OPP and OVP resistors. See APPENDIX 2 .

The electrical schematic (APPENDIX 2) shows an additional OPP circuit, circuitry around Q7104 and Q7105, which can be used in case UVLO detection is jeopardised by peak rectification on the auxiliary winding. Information of the feedback loop is used to detect an over power condition.

3.9 DRIVE CIRCUITRY

The drive resistor can be estimated using the average drive current of the TEA1533 driver stage (linear approximation)

$$i_{drive} = \frac{C_1\left(V_{th} + i_{drive}R_{drive}\right) + dQ + C_2\left(\Delta V + i_{drive}R_{drive}\right)}{t_{sw\_on}},$$

(3.30)

in which C_1 and C_2 are the equivalent gate source capacitors, dQ is the change of gate charge at the threshold level and ΔV is the gate voltage level higher than the threshold level. Solving for the drive resistor leads to

$$R_{drive} = \frac{t_{sw\_on}}{C_1 + C_2} - \frac{C_1 V_{th} + dQ + C_1 \Delta V}{i_{drive}\left(C_1 + C_2\right)}.$$

(3.31)

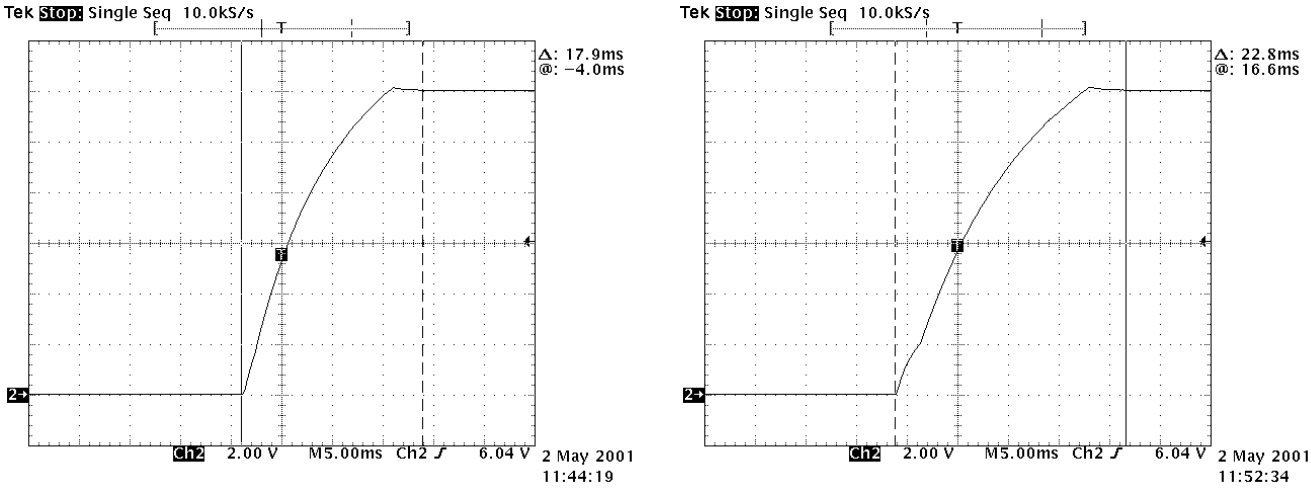
Were $i_{drive} = 125\text{mA}$. Substituting the data from the datasheet and assuming a minimum switch on time of 100ns results in $R_{drive} = 28\Omega \rightarrow R_{drive} = 22\Omega$.

Additional components (diode and resistor) are included in the PCB layout to tailor the drive in case of EMI problems or high switch “off” losses.

4. MEASUREMENTS

4.1 OUTPUT VOLTAGE

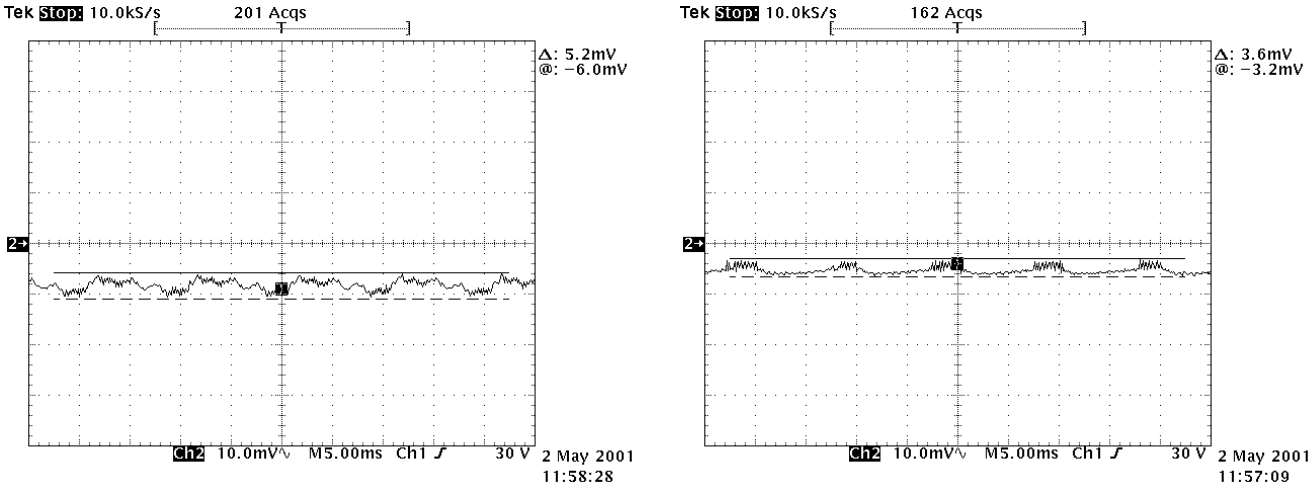
4.1.1 Start-up time



(a) *(b)*

Fig. (4.1) The output voltage start-up behaviour at maximum load (a) V_{ac}=110V (b) V_{ac}=230V

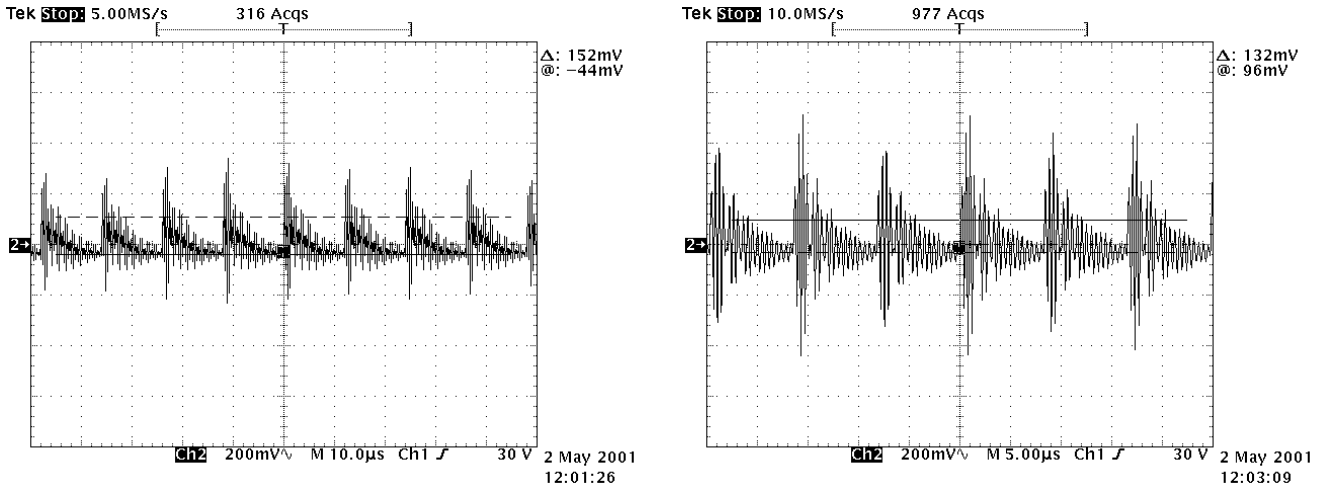
4.1.2 Line regulation



(a) *(b)*

Fig. (4.2) The influence of the line voltage ripple on the output voltage at maximum load (a) Vac=110V (b) Vac=230V.

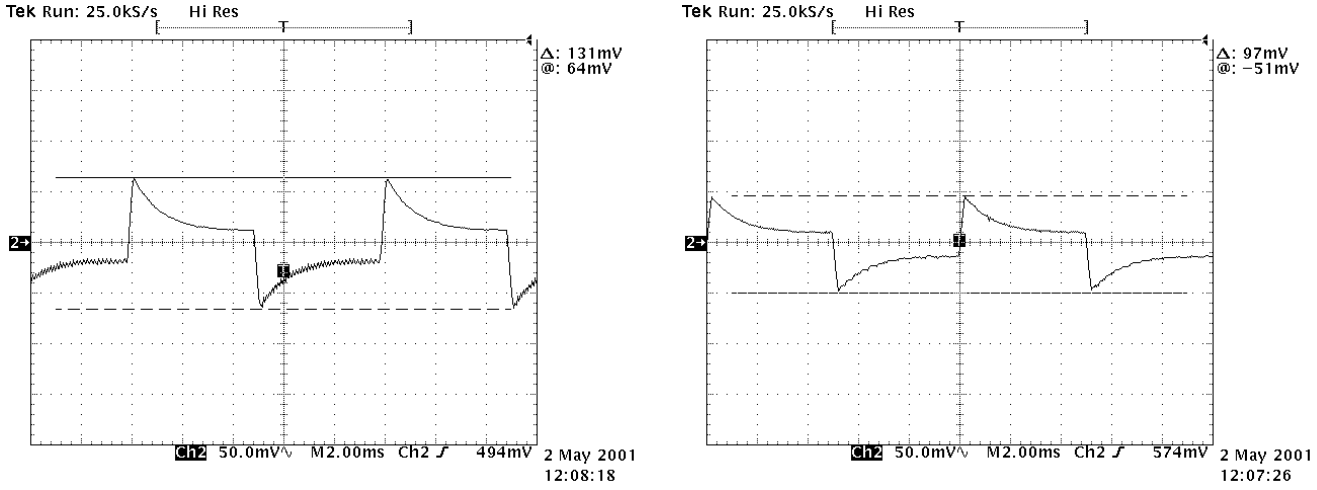
4.1.3 Output ripple



(a) *(b)*

Fig. (4.3) Output voltage ripple at maximum load (a) Vac=110V (b) Vac=230V.

4.1.4 Step response



(a) *(b)*

Fig. (4.4) Output voltage response to an alternating output current of 200mA…4A@100Hz (a) Vac=110V (b) Vac=230V.

4.2 ELECTRICAL COMPONENT STRESS

4.2.1 Primary MOSFet

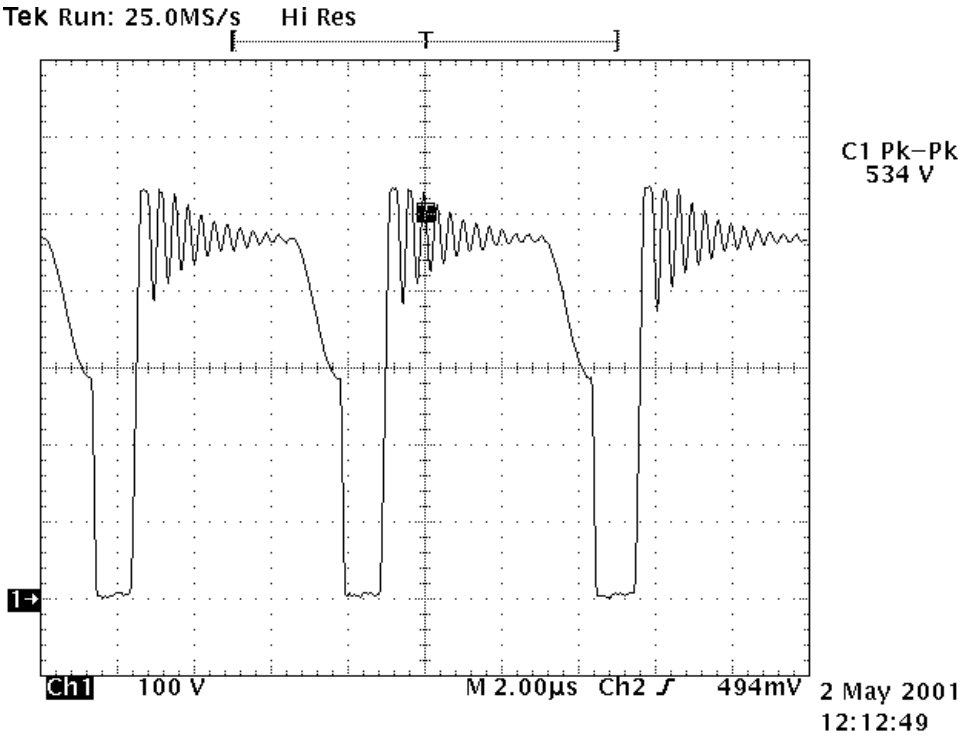
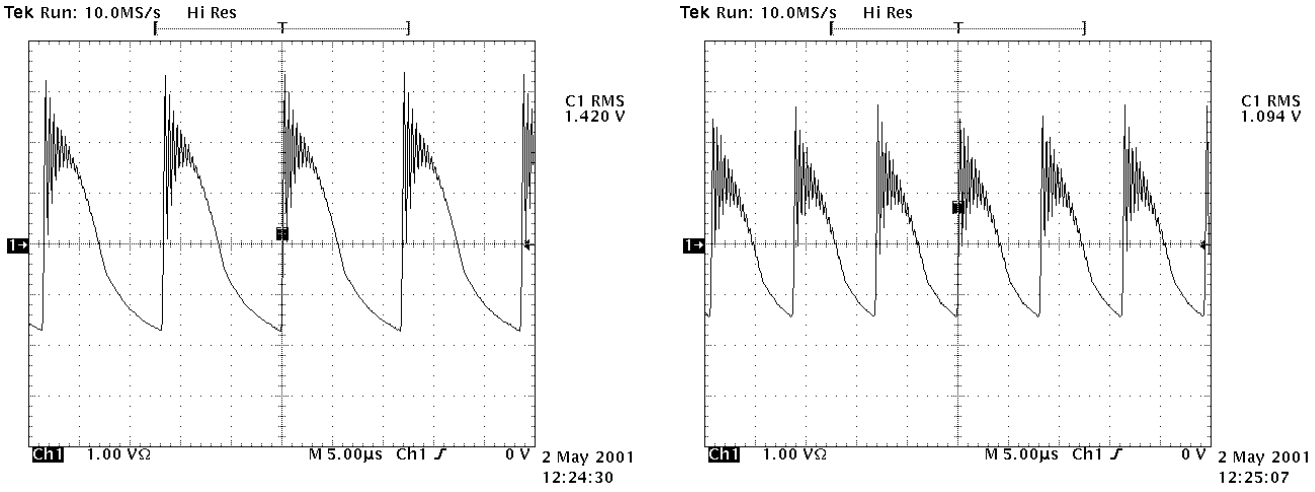


Fig. (4.5) Maximum drain voltage level at V_{ac}=264V and I_o=4A.

4.2.2 Secondary Capacitors



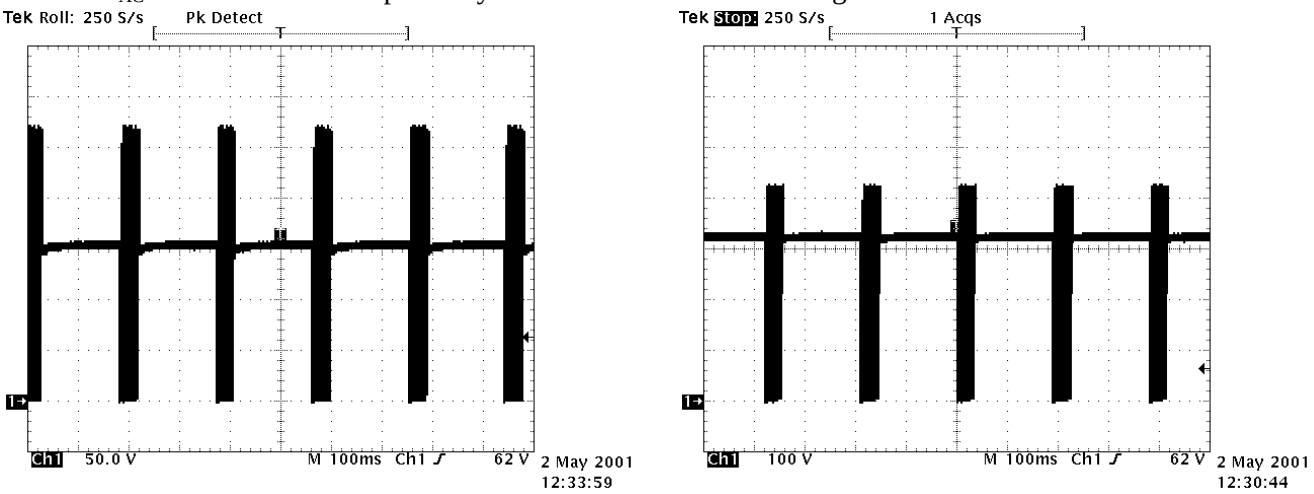
(a) *(b)*

Fig. (4.6) The secondary capacitor current (a) Vac=110V (b) Vac=230V.

4.3 PROTECTIONS

4.3.1 Over power protection

Fig. (4.7.a) and Fig. (4.7.b) show the drain voltages during the burst mode. The power consumption at $110V_{AC}$ and $230V_{AC}$ is 3W and 2.4W respectively which are well below the target of 5W.



(a) *(b)*

Fig. (4.7) The drain voltage at a short-circuited output (a) Vac=110V (b) Vac=230V.

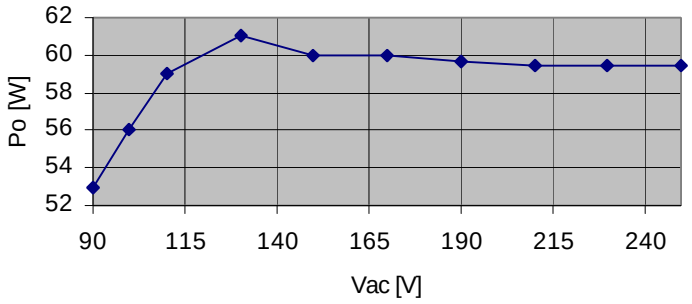
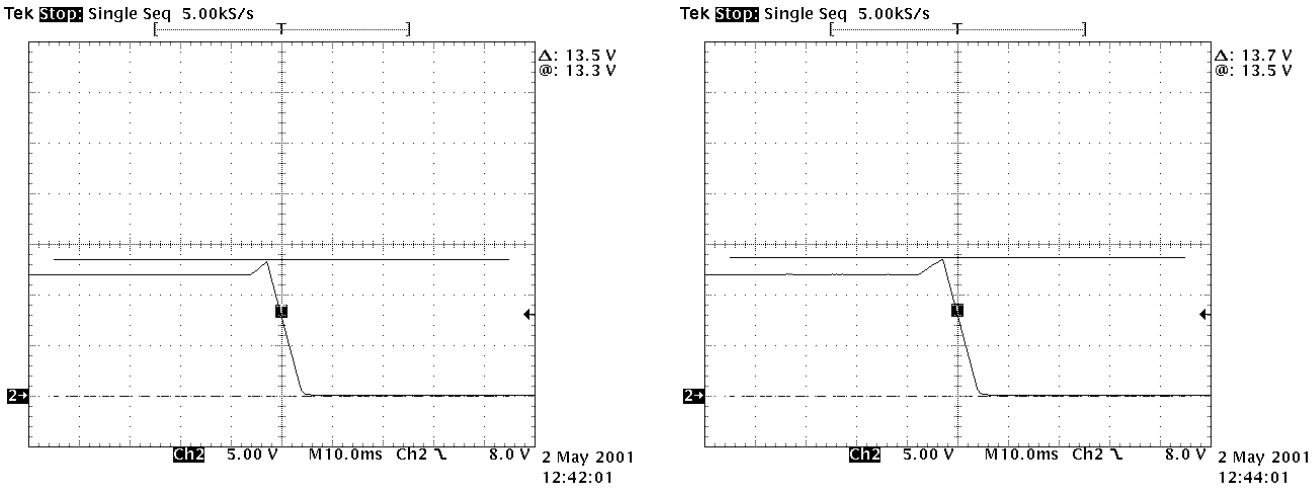


Fig. (4.8) The Over Power Protection level as function of the mains voltage.

4.3.2 Open Loop Protection (Over Voltage Protection)



(a) *(b)*

Fig. (4.9) Output voltage behaviour under open loop test condition (a) Vac=110V (b) Vac=230V.

4.4 EFFICIENCY AND POWER CONSUMPTION

4.4.1 Efficiency

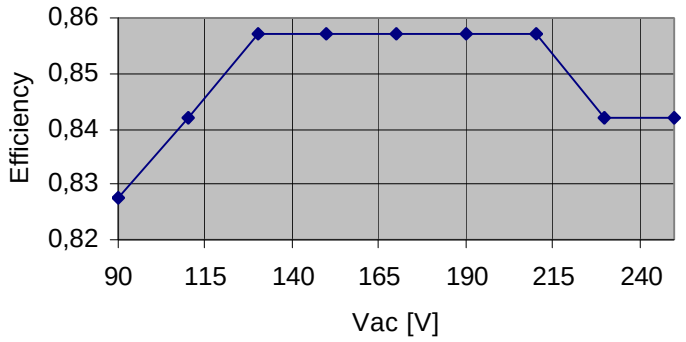
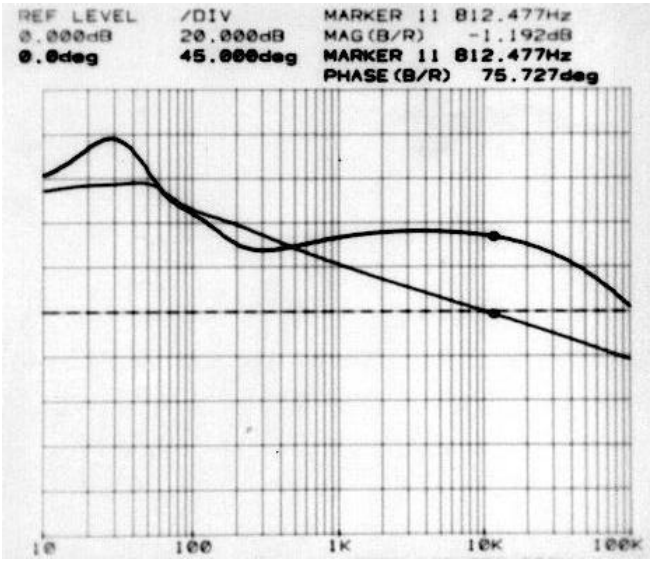


Fig. (4.10) The efficiency as function of the input voltage at maximum output power

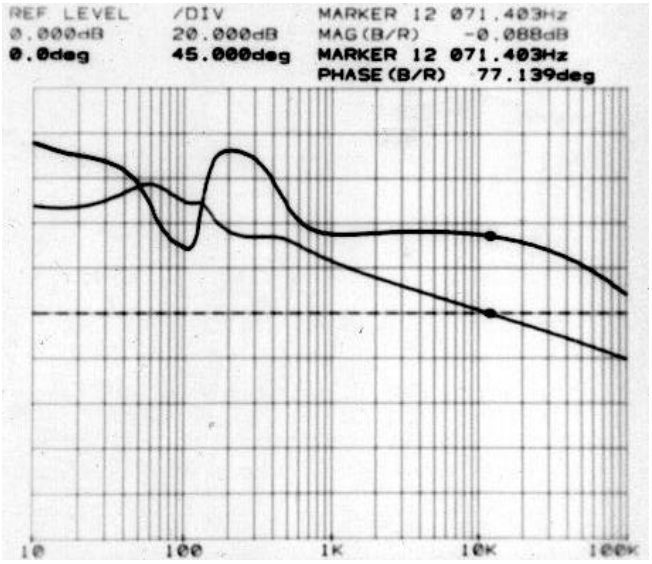
4.4.2 Standby Power

V_{ac}	P_{in} (no load)	P_{in} (P_o=150mW)
110V	252mW	590mW
230V	297mW	660mW

4.5 GAIN – PHASE CONTROL LOOP



(a)



(b)

Fig. (4.11) Phase - Gain (a) Vac=110V (b) Vac=230V.

4.6 EMC

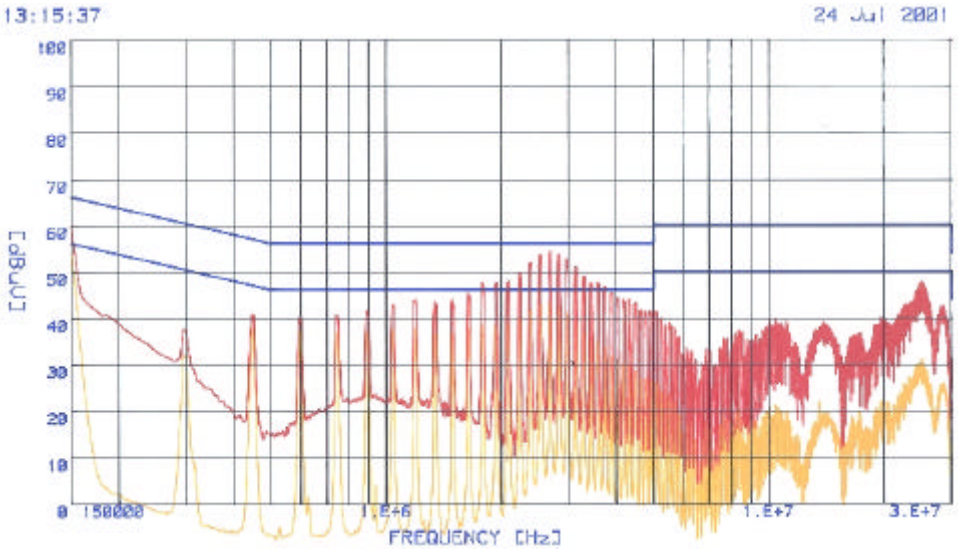


Fig. (4.12) Disturbance at mains input measured in accordance with CISPR 13 and CISPR 22.

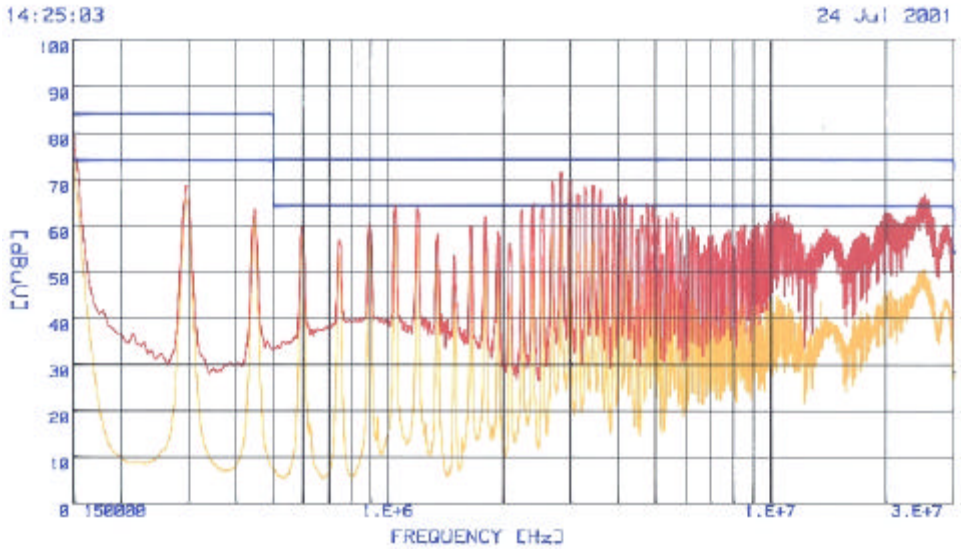


Fig. (4.13) Disturbance at 12V output measured in accordance with CISPR 13 and CISPR 22.

4.7 TEMPERATURE STRESS

Temperature measurements are done for the most concerned components. The results for low and high mains are given in Table 4.1and.Table 4.2

V_{AC}=110V_{ac}, i_o=4A	
T_{diode_sec}	60
T_{MOSFet}	60
T_{trafo_Cu}	56
T_{trafo_Fe}	52
T_{elco_sec}	37
T_{amb}	24

Table 4.1 Temperature measurements of critical components

V_{AC}=230V_{ac}, i_o=4	
T_{diode_sec}	69
T_{MOSFet}	79
T_{trafo_Cu}	62
T_{trafo_Fe}	57
T_{elco_sec}	37
T_{amb}	24

Table 4.2 Temperature measurements of critical components

APPENDIX 1 SPECIFICATION

1. INPUT

- Input voltage range : 90…264V_{AC}
- Line frequency range : 50/60Hz±3%
- Inrush current at 25^{0}C : 25A maximum at 120V_{AC}
  50A maximum at 240V_{AC}
- Input current : 1A_{rms} max.

2. OUTPUT

- Output voltage : 12V_{DC}±4%
- Ripple and Noise : 120mV_{pp}
- Output current : 4A max.

3. Efficiency

- >83% (including power losses in input filters) at maximum load

4. Protections

- Over Power Protection (OPP) : 150% of P_{omax}, auto restart
- Over Voltage Protection (OVP) : 15V_{DC} max, auto restart
- Short Circuit Protection (SCP) : Auto restart type, P_{loss} < 5W

5. **Soft start** : The system must start up gradually within 100ms

6. Hold up time

- 10ms minimum at 100V_{AC} input voltage, maximum output load.

7. Insulation resistance

- Input to output : 100MΩ minimum at 500V_{DC}
- Input to ground : 100MΩ minimum at 500V_{DC}

8. Printed circuit board

- Technology : single sided FR2
- Dimensions : 150mm (L), 100mm (W) and 20mm (H)

9. Environment

- Operation temperature : 0…40^{0}C
- Operation humidity : 10…90% RH
- Storage temperature : -20…60^{0}C
- Storage humidity : no condensation

10. Green functions

- Less than 1W at 100mW output power
- Less than 300mW at no load

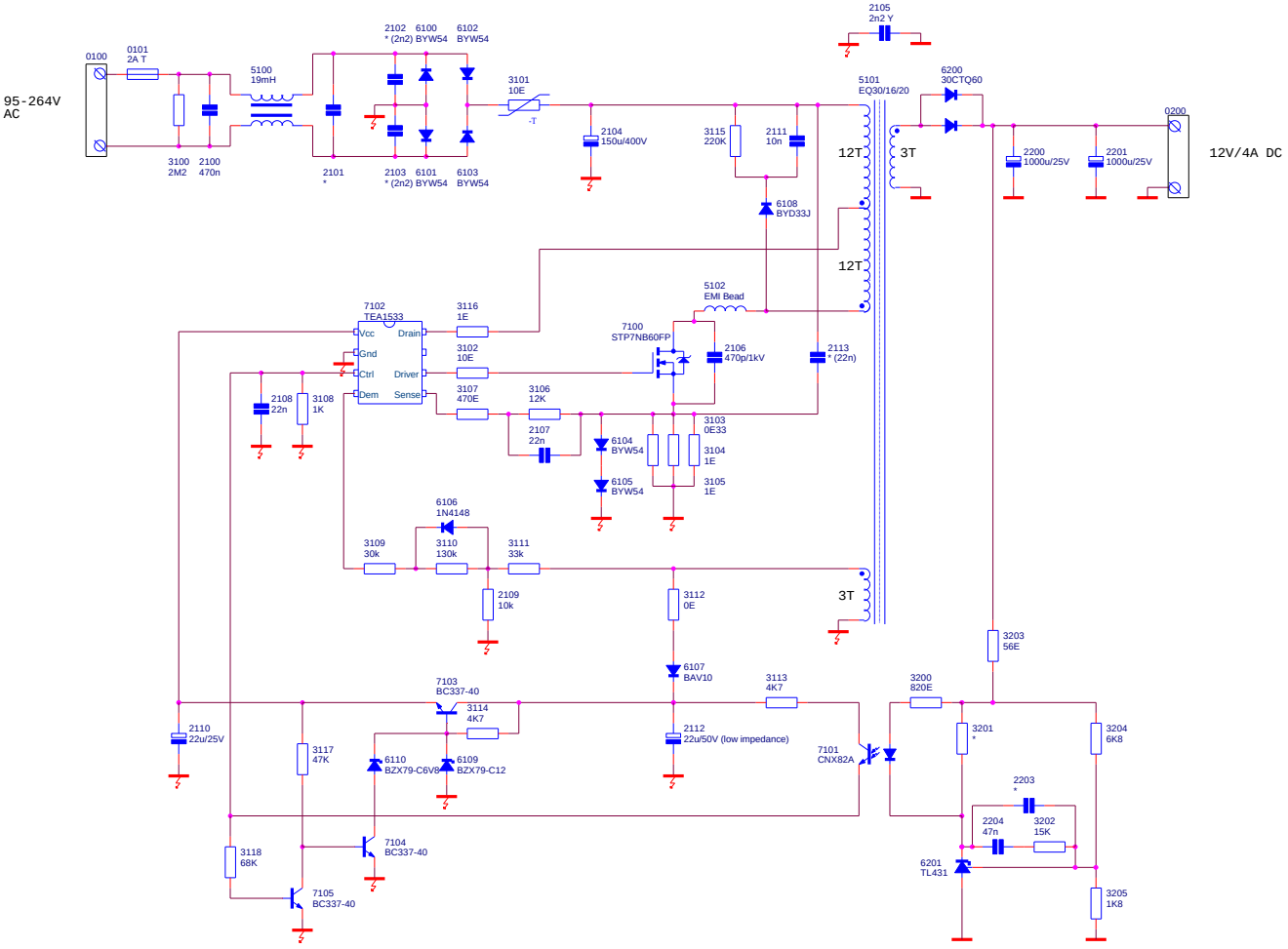
11. Safety requirement

- Meet international standards

12. EMI requirement

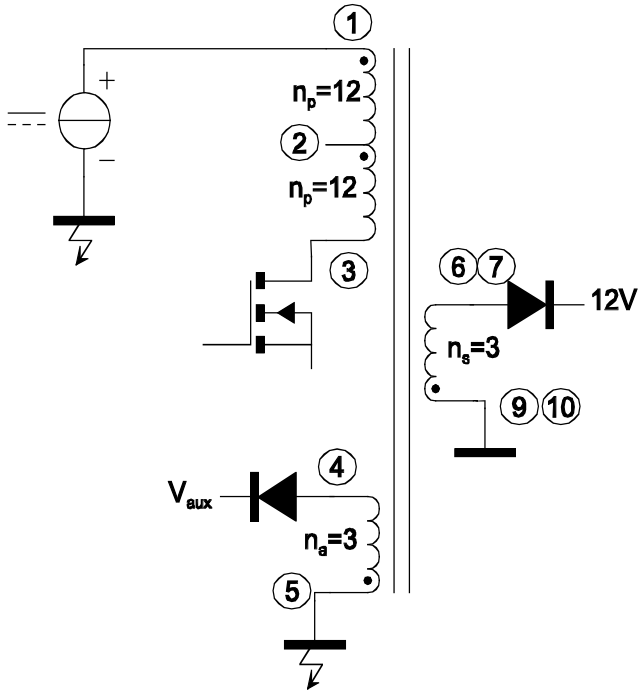
- Meet international standards

APPENDIX 2 ELECTRICAL SCHEMATIC



Components marked with *
are reserved components

APPENDIX 3 TRANSFORMER SPECIFICATION



This EQ30 type transformer (part number 70A-1001B) is supplied by Delta Electronics Inc. For any questions or information about this transformer, please contact

Delta Contact Person - Tina Tien
Delta Electronics , INC.
E-mail :tina.tien@delta.com.tw
Tel:886-3-3626301ext656
Fax:886-3-3618901